

PREDICTIVE FAILURE MODEL FOR FLIP CHIP ON BOARD COMPONENT
LEVEL ASSEMBLIES

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PREDICTIVE FAILURE MODEL FOR FLIP CHIP ON BOARD COMPONENT
LEVEL ASSEMBLIES

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1 INTRODUCTION

1.1 Industry Needs

The electronic packaging industry is predicted to generate \$32 billion in revenue by 2004, approximately 10% of all semiconductor revenue. The packaging industry as a whole is a \$125 billion worldwide market, employing more than a million people. Electronic packaging is the method by which an integrated circuit is packaged in a modular form so that it can be used in an end product; a cell phone, a lap top computer, or even a smoke detector. The integrated circuit has been traditionally connected to the interposer with an array of gold wires. The interposer is the circuit board between the integrated circuit and the final circuit board assembly. In recent years, there has been a shift from wire bonded integrated circuits to flip chip interconnect structures. Flip chips use an array of small solder bumps to distribute the electrical signal from the silicon to the interposer, instead of the gold wires previously used. This shift in packaging technology resulted in smaller components with improved electrical and thermal performance. With these improvements comes concern about reliability performance, a new component level interconnect structure comes with a unique set of reliability challenges. The reliability of flip chip components is assessed with environmental stress tests, or accelerated life tests, which apply stresses to electronic packages that exceed the stress levels experienced in the field. This reliability testing of flip chip components takes time, money, and a significant amount of capitol equipment. The focus of this research is to develop a predictive methodology for determining thermal cycling performance, and to understand the affect of process-induced defects on reliability

performance. To accomplish this goal a strain based fatigue equation will be generated via analytical, computational, and experimental techniques. This model differs from others because it incorporates the effects of process-induced defects as well as factors that are difficult to model analytically such as solder joint shape and the glass transition temperature of the underfill material.

1.2 Flip Chip Technology and Terminology

A schematic of a flip chip component is shown in Figure 1-1. The term flip chip refers to the method of attachment of the active silicon, or the integrated circuit, to the next level of assembly. Bumps are applied to the silicon to make a flip chip, then the chip is ‘flipped’ and placed on the interposer, and all solder interconnects are formed simultaneously in a thermal oven, or Reflow oven. A polymer, called underfill, can be applied between the silicon and the interposer to improve reliability performance of the component (this is not shown in Figure 1-1). This underfill material is needed because there is a large difference in the coefficient of thermal expansion (CTE) between the silicon and the interposer. Because of this thermal expansion mismatch, the flip chip solder joints experience fatigue damage during thermal cycling or power cycling. This research proposes an analytical physics based model for the prediction of cycles to failure of the flip chip solder joints.

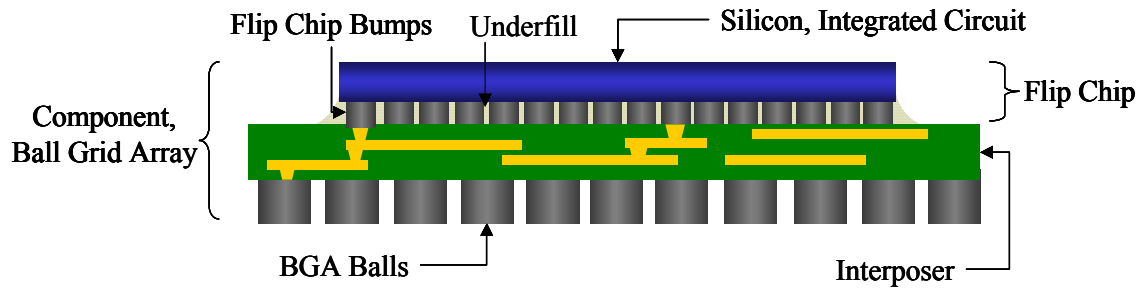


Figure 1-1 Schematic of Flip Chip Component and Terminology

1.3 Summary of Research

To determine the reliability performance of electronic components, environmental stress tests, or accelerated life tests, are used to apply stresses to electronic packages that exceed the stress levels experienced in the field. In theory, these elevated stress levels are used to generate the same failure mechanisms that are seen in the field, only at an accelerated rate. Unfortunately, it is well known that reliability testing is not a foolproof method of failure mode screening. The methods of assessing the reliability performance of electronic packages can be classified into two categories: a statistics based approach and a physics of failure based approach. This research will use a statistics based methodology to identify the critical factors in reliability performance of flip chip on board component level assemblies and a physics of failure based approach to develop a low cycle strain based fatigue equation for flip chip component level assemblies via a correction factor approach. The critical factors in determining reliability performance will be established via experimental investigation and their effect quantified via regression techniques. This methodology differs from other strain based fatigue approaches because it will not be an empirical fit to experimental data; it will incorporate

regression analysis results and the underlying physics of failure into correction factors for a low cycle strain based fatigue equation. The end product will be a general equation rather than one that is specific to a certain test vehicle or material set. In addition, this methodology could be used to generate correction factors, or correction functions, for various parameters that are difficult to model via computational finite element methods; substrate metallization and the possibility of gold embrittlement would be a good example of the this type of predictor.

Several experimental test vehicles are necessary for the regression analysis of input parameters and the response variable, mean time to failure, MTTF. The test vehicles all use square daisy chain test die, no flow underfill and organic substrates. All test vehicles will be electrically testable daisy chain structures; a simple continuity test will be used to determine if the integrity of solder joints has been compromised. Once a component level assembly fails electrically, it will be removed from testing and various failure mode analysis techniques will be used to determine the root cause of failure; x-ray imaging, scanning acoustic microscopy, cross sectional analysis, and scanning electron microscopy. The reliability testing results for AATC and LLTS will result in failures times that were arbitrarily censored; right censored and interval censored. The samples were interval censored because the exact number of cycles to failure was not obtained since resistance measurements were taken every 100 cycles; in addition, if parts were removed from test prior to failure to inspect for cracks or solder extrusion they would be right censored data points. Acceleration factors will be calculated from the failure data for the various component level structures and the influence of various input parameters will be determined via regression analysis. Input parameters that will be investigated are

die size, substrate metallization, underfill voiding as a percentage of total area, mask defined vs. copper defined pad structures, material properties of the underfill, substrate bond pad area vs. UBM area, and bump layout. All dominant factors from the regression analysis will be incorporated into a strain based fatigue equation for flip chip on board component level assemblies, generating a general flip chip on board strain based fatigue equation that is not test vehicle or material set specific.

Finite element modeling will provide the necessary tool to evaluate several strain based fatigue equations as well as check the validity of the proposed flip chip on board strain based fatigue equation. Finite element modeling will serve as the ‘control’ method for predictive failure modeling and the results of the final strain based fatigue model will be compared against the FEM output and experimental results.

1.4 Thesis Structure

Chapter 2 presents a literature review covering basics on reliability modeling and common parametric distributions that are used to describe failure rates for electronic components. Chapter 3 outlines the scope and objectives of this work. Chapter 4 provides (1) a detailed description of the test vehicles used for the determination of correction factors in the final strain based fatigue model and (2) an outline of the methodologies used for finite element modeling. Chapter 5 gives the analytical model development and presents a low cycle strain based equation with correction factors for underfill glass transition temperature, solder joint shape, and substrate metallization. Chapter 6 outlines AATC and HTS reliability results. Chapter 7 provides a short case

study to show the utility of the model and validate the model for a new component level package structure with new underfill materials. Chapter 8 provides conclusions, contributions and recommended future work. Appendix A outlines the APDL code that was used for the finite element modeling in ANSYS and Appendix B provides a step by step illustration of the final model generation via regression analysis.

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2 LITERATURE REVIEW

2.1 Flip Chip Process

Flip chip technology was originally invented by Bell labs and implemented by IBM over 30 years ago. Other interconnection methods such as wirebonding have been used for years, and the current component assembly infrastructure supports these interconnection methods. A brief summary of flip chip technology and the current flip chip assembly processes will be discussed in this section.

2.1.1 Flip Chip Attachment

The name ‘flip chip’ refers only to the method of attaching the die to the next level of interconnect. The first flip chips were developed in the early 1960s to reduce the expense and low throughput of manual wire bonding. Wire bonding requires the ‘active’ side of the die to be face-up, this is opposite that of a flip chip, and wires are run from the active terminals to the next level of interconnect. Flip chip technology, however, inverts the chip and all terminal contacts are made simultaneously via the reflow soldering process. Attractive characteristics of flip chip technology are: high performance, short interconnections, fast signal distribution, and low cost—ideal for next generation applications. One of the greatest advantages in using flip chip technology in surface mount technology is the chip’s high I/O density compared to traditional surface mount devices. Surface mount technology describes the method by which electrical components are attached to the surface of a printed wiring board. SMT was the fastest growing technology in consumer electronics in the early 1980s. In general, the packages for SMT

can be developed with pads or connections out of the packages at tight spacings; this means that more components can be placed on each printed wiring board [Tummala, 1997]. The performance and functionality of a chip increases as the as the number of solder bumps under the silicon increases. As with all new technology, there are always trade-offs. For instance, with this increased performance one might sacrifice reliability with the silicon to substrate interconnections. There are various issues with flip chip processing that need to be addressed and understood before implementing flip chips into an electronic assembly.

2.1.2 Low Cost Flip Chip Process

The low-cost flip chip process is illustrated in Figure 2-1.

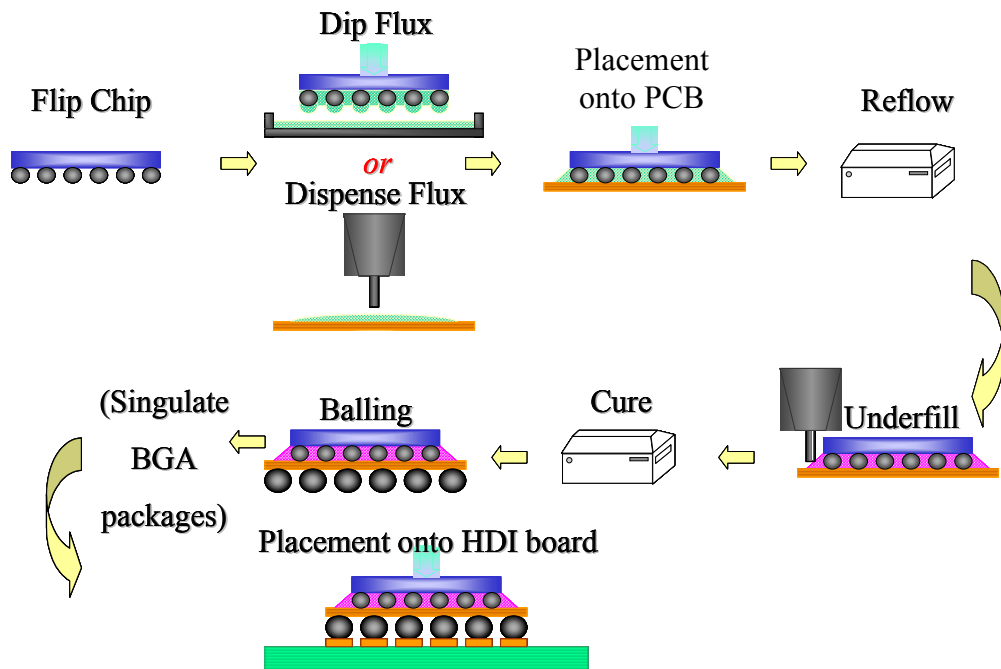


Figure 2-1 Low Cost Flip Chip Process-Capillary Flow Underfill

The first step in flip chip processing is a fluxing operation. Flux is a material that promotes solder-to-substrate wetting, removes oxides from the bonding surfaces, and protects the surfaces against further oxidation during the reflow soldering process. Flux can be applied either by dipping the flip chip into a level flux bath or flux can be dispensed onto the actual substrate bond sites. Once the flux is applied to the wettable surfaces the chip is placed onto the substrate—both the flux application and the placement of the chip are carried out in the placement machine. This assembled chip is then reflowed in a forced convection reflow oven. During the reflow process the flux is activated, and it proceeds to clean and reduce all wettable surfaces and prevents the surfaces from re-oxidizing. Next the tin-lead solder bumps become molten and wet to the substrate pads. All solder connections form simultaneously when the reflow temperature drops below 183 °C (the melting temperature of the eutectic solder). The next step is to dispense underfill and an epoxy-based material to fill the gap between the chip and the substrate. The underfill is then cured in a thermal chamber at a given temperature for a given duration of time. The underfill manufacturer usually supplies the specific curing recipe.

Another flip chip process flow involves the use of no-flow underfill (Figure 2-2).

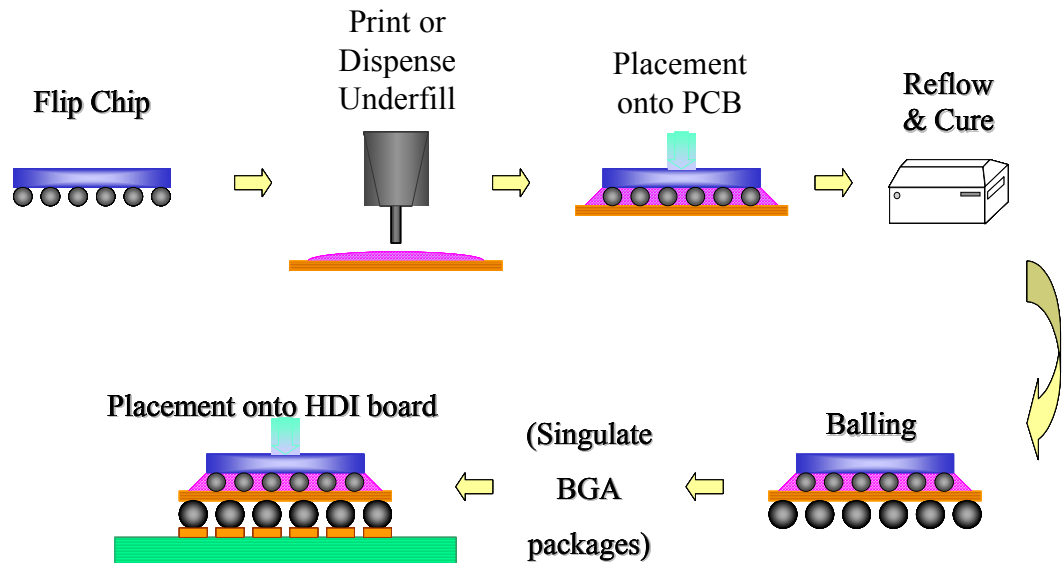


Figure 2-2 Low Cost Flip Chip Process – No-Flow Underfill

No-flow underfill is an attractive option because it greatly reduces the amount of processing steps, and therefore, the processing time needed. The no-flow process typically begins with the dispense or print of no-flow underfill onto the center of the chip bond area. The flip chip is then placed in the middle of this area compressing the underfill deposit and allowing the flip chip bumps to make contact with the substrate bond pads. The assembly is placed in the reflow soldering oven where all necessary solder connections are made between the flip chip and the substrate. It is important to note that some types of the no-flow underfills require a post-reflow cure at an elevated temperature for a given amount of time, this would be designated by each individual underfill manufacturer.

2.2 Materials used in Flip Chip Assembly

The materials used in flip chip assembly are slightly different than the materials used in standard surface mount assembly. Namely, flux and underfill are used instead of solder paste to adhere the component, in this case a flip chip, to the next level of interconnect. The materials themselves, flux and underfill, must be considered as well as their interaction with one another. This interaction can affect everything from underfill curing times to reliability performance. Flux, underfill, and flux-underfill compatibility will be discussed in this section.

2.2.1 Flux

Fluxes are organic or synthetic materials used in electronic assembly to remove oxides from wettable surfaces (die bumps as well as substrate pads) and to improve solder wetting in the reflow soldering process. There are two main types of flux used in industry today: water soluble flux and no-clean flux. Water soluble flux leaves an unacceptable amount of solid flux residue on the substrate and die after it has been processed. These residues must be removed via a post-reflow cleaning operation; this is important because flux residues are often not compatible with underfills. This incompatibility will often times result in underfill delamination when components are placed in accelerated life testing. No-clean flux does not require this additional processing step, and therefore results in lower cost and higher throughput. There are two types of no-clean fluxes used for flip processing and assembly. The first is a tacky flux, which is adhered to the bumps of the die prior to assembly via a dipping process. The dip

height and the amount of flux is controlled by the height of the flux in the dip fluxing film/bath. One way to achieve the flux film is using a rotating disk and a doctor blade configuration. The disk is spun after each part has been dipped ensuring that the next part that is dipped will have the same amount of flux applied to it. The second no-clean flux application is a dispensing process. A flux that can be dispensed is a much less viscous material that can be either sprayed or dropped onto the substrate prior to die placement.

2.2.2 Underfills

Underfill is required to relieve the CTE (coefficient of thermal expansion) mismatch between the silicon chip and the substrate. Underfills are used to reduce the strain on the solder joints resulting in significant improvements in interconnect fatigue life [Suryanarayana D., et al. 1991]. Eutectic flip chip packages with underfill have a reliability 15 times longer than those packages without underfill. This is because the underfill provides the necessary chemical affinity and serves as the mechanical lock that keeps the entire assembly in tact [Patterson, et al., 1997]. Underfill is polymer adhesive material (often times an epoxy based material) that fills the gap between the bottom of the chip and the top of the substrate. Standard capillary flow underfills and fast flow snap cure underfills are filled with silica particles or fused silica. No-flow underfills are void of any such particles. The fast flow snap cure and standard capillary flow underfills are dispensed along the edge of the chip and allowed to flow under the chip via the capillary flow of the liquid underfill. This flow is initiated by the underfill surface tension and the pressure difference [Baldwin, 1997].

2.3 Reliability Tests

The reliability of an item is defined as the probability that it will adequately perform its specified purpose for a specified period of time under specified environmental conditions [Leemis, 1995]. In the specific case of microelectronics assembly, the ‘item’ is an electronic package, ‘adequately performs’ is the given set of acceptable operating levels set by the experimenter, and the ‘specified period of time’ and ‘environmental conditions’ are set by the actual test that is being performed (i.e. number of cycles, temperature, and humidity levels). The reliability of a component should not be confused with the quality of a component—reliability incorporates the passage of time while quality does not.

The hazard function is a very popular method used in lifetime modeling. Although this method might assume several different names in literature, it is simply the ratio of the probability density function to the survivor function. The survivor function is the probability that a component is functioning at any time, t .

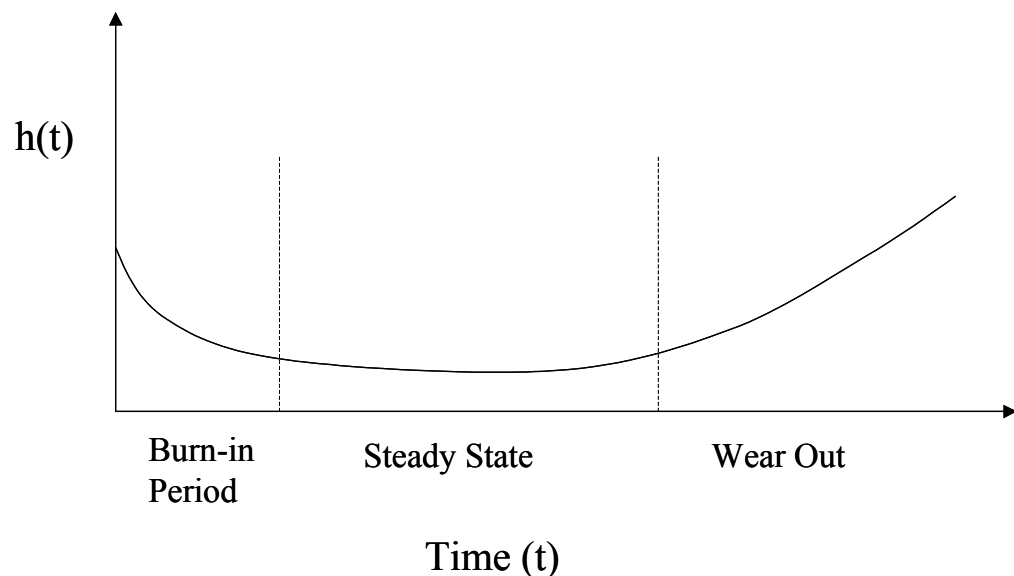


Figure 2-3 Bathtub hazard function

Testing done at the manufacturing facility usually catches failures in the burn-in period. Once the item passes the early part of its life, it sustains a fairly steady state hazard function. Its reliability is therefore constant. Finally, as components continue to age, the hazard function increases without limit, resulting in wear-out failures [Leemis 1995].

Several reliability tests were used during different stages of our experimentation with different response variables measured. The following sections will discuss the specifics of commonly used accelerated life tests.

2.3.1 J-STD-020A

The purpose of this IPC JEDEC standard is to identify the classification level of nonhermetic solid state Surface Mount Devices (SMDs) that are sensitive to moisture-induced stress so they can be properly packaged, stored, and handled to avoid subsequent thermal/mechanical damage during the assembly solder reflow attachment and/or repair operation [J-STD-020A, 1999].

In general, the JEDEC procedure requires assembly of at least 11 substrates from three nonconsecutive assembly lots. These substrates then must go through a battery of initial tests to prove that the assembly process was adequate and to determine the substrates pre-testing condition. The substrates are electrically tested, visually inspected, and examined via an acoustic microscope for any internal cracking or delamination. The substrates are then baked at 125°C for 24 hours and placed into a temperature humidity chamber for a specified number of hours. The number of hours

and the temperature and humidity levels are established based on the JEDEC level that is being verified. There are also accelerated equivalents for many of the levels. Once the components have finished the temperature humidity they are reflowed three times per the JEDEC reflow specification. All samples are then examined for cracks and delamination. Failure criterion is detailed in the JEDEC specification.

2.3.2 Temperature Cycling

The purpose of temperature cycling is to expose the component level package to high as well as low temperature extremes. This method of testing accelerates the failure mode caused by cyclic stresses; these stresses are imparted by transitioning the part from a high to a low temperature and visa versa. This test was an important one for the experimentation because of the large CTE mismatch between the silicon flip chip and the FR4 substrate. In general, there are two types of temperature cycling tests: thermal shock and thermal cycling. The main difference in these tests is the physical chamber used for testing, many thermal shock tests are conducted with two separate liquid thermal baths or separate air chambers where the components being tested are shuttled between a hot bath and a cold bath. These thermal shock tests often generate very high ramps rates for the components that are being tested. A thermal cycle test is often conducted in a single air chamber where the temperature ramp rate can be carefully controlled. The air-to-air testing uses air filled chambers at different temperatures and the liquid-to-liquid test used liquid chambers at different temperatures. Liquid-to-liquid and air-to-air test conditions can be found in JESD22-A106-A and JESD22-A104-A specifications respectively.

2.4 Reliability Prediction Methods

There have been increased demands in terms of quality for almost all consumer products including; automotive electronics, consumer electronics, military equipment, and equipment needed for space exploration. These increased demands on quality directly impact the quality assurance and quality prediction methods of the independent component and raw material manufacturers for years to come. These trends point to a need to improve tools and techniques for reliability analysis at a very early stage in the design process. In this section, the traditional approaches for reliability analysis at a system and individual component level will be discussed in addition to any shortcomings with the current methodologies. Reliability prediction methods can be divided into three main areas: statistical modeling, Finite Element Modeling (FEM), and Physics of Failure (PoF) based modeling. These will be discussed in detail; however, it is appropriate to define Reliability and Quality in a rigorous sense.

2.4.1 What is Reliability and What is Quality

In the general sense, reliability is defined as *the ability of an item to perform a required function under stated conditions for a stated period of time* [Bajenescu, Bazu 1999]. The *stated conditions* include the actual field environment this encompasses the mechanical, electrical, and thermal conditions for an electronic package. *Perform* means that the component is capable of functioning at an acceptable level, i.e it does not fail. Finally, the *stated period of time* is the desired amount of time that a component must *perform* in

the field. This time period will vary greatly depending on the product, for example the computer in your car is expected to last at a minimum 3 years or 36K miles, however consumers typically expect their cell phones to last a year or so before they upgrade to the next free phone provided by their service provider. Therefore, the time period is largely defined by the field use condition and customer needs, this will be discussed in detail in the following sections.

Quality is the condition that makes an object or a functional element correspond to the pre-established requirements [Bajenescu, Bazu 1999]. These *pre-established requirements* can usually be found in a warranty agreement, and they are typically listed as a failure percentage at a given use lifetime or a given amount of hours of operation. Also, it should be mentioned that the primary difference between the term *quality* and the term *reliability* is that reliability incorporates the passage of time while quality does not, since it is a static descriptor of an item [Leemis, 1995].

2.4.2 Statistical Prediction Methods

Let's move into a statistical definition of reliability. Initially there are n_o identical components subjected to a generic stress test. During the testing time interval $(t-\Delta t, t)$, there are $n_f(t)$ failed components and $n_s(t)$ survived components, so at any given point in time $n_f(t)$ and $n_s(t)$ add to get n_o . Reliability is defined at the cumulative probability function of success (or the probability that the component has not failed by time t), and then reliability as a function of time is [Elsayed, 1996]:

$$R(t) = \frac{n_s(t)}{n_s(t) + n_f(t)} = \frac{n_s(t)}{n_o} \quad (2-1)$$

The reliability is sometimes also referred to as the survival function. So, if t' is a random variable denoting the time to failure, then the reliability function at time t can be denoted as

$$R(t) = P(t' > t) \quad (2-2)$$

The cumulative distribution function of failure $F(t)$ is the complement of reliability $R(t)$, meaning that $F(t)$ and $R(t)$ sum to 1. If the time to failure, t' , has a probability density function $f(t)$, then we can express the reliability in terms of the probability density function for any given failure distribution. For the purposes of illustration the exponential function will serve as a straight forward example, with a constant failure rate. The probability density function for the exponential distribution is:

$$f(t) = \lambda e^{-\lambda t} \quad (2-3)$$

Such that the reliability function is then;

$$R(t) = 1 - \int_0^t \lambda e^{-\lambda \beta} d\beta = e^{-\lambda t} \quad (2-4)$$

The probability of failure of a component in a given time interval $[t, t + \Delta t]$ expressed in terms of the reliability function is:

$$\int_t^{t+\Delta t} f(t) dt = R(t) - R(t + \Delta t) \quad (2-5)$$

The failure rate during a time interval is the probability that a failure per unit time occurs in the interval given that no failure has occurred prior to t , which is the beginning interval. Therefore the failure rate can be expressed as:

$$\frac{R(t) - R(t + \Delta t)}{\Delta t R(t)} \quad (2-6)$$

Finally, the instantaneous failure rate or the limit of the failure rate as Δt approaches zero is defined as the hazard function.

$$h(t) = \lim_{\Delta t \rightarrow 0} \frac{R(t) - R(t + \Delta t)}{\Delta t R(t)} = \frac{f(t)}{R(t)} \quad (2-7)$$

It is a good time to mention that the plot of the hazard rate, $h(t)$, as a function of time will result in the well known ‘bathtub’ curve that is seen so often in microelectronics reliability with each point corresponding to the instantaneous failure rate of a component. The bottom of the bathtub curve is basically a horizontal line which represents a constant failure rate while in a use environment; any failures that occur in this region are intrinsic failures that are a result of design, material selection, or potentially the use environment. Failures that occur prior to this constant failure rate are early life failures and are usually removed prior to reaching the customer, through a burn-in test done at the manufacturer. A burn-in test is basically a test run at a slightly higher stress level than the operating levels to weed out any potential early life failures. Finally, after the constant failure rate there is a sharp increase in the frequency of failures which are referred to as end of life failures or wear out failures.

The above description basically outlines a general explanation of reliability of a single component, however, often times an engineer might be concerned with the

reliability of a system. If the failures of the components are statistically independent and the structure of the system is serial in nature, meaning there are no redundant components, the system reliability can be expressed as

$$R_{sys} = R_1 \cdot R_2 \cdot R_3 \quad (2-8)$$

The reliability of the individual components in a system are multiplied together to give the total reliability of a system.

2.4.2.1 Mean Time to Failure

The mean time to failure (MTTF) is the expectation of the time to failure T and can be written as [Hayter 1996]

$$E(T) = \int_0^{\infty} tf(t)dt \quad (2-9)$$

The mean time to failure for the exponential distribution is $1/\lambda$, or the inverse of the scale parameter. The exponential distribution is useful for many reliability calculations. It represents a constant failure rate and therefore is useful in describing the intrinsic failures throughout the life of a component; recall that this is the failure rate seen by the end consumer throughout the life of the product. In addition, the exponential distribution simplifies many mathematical calculations.

The mean time to failure for the Weibull distribution is:

$$MTTF_{weibull} = E(T) = \frac{1}{\lambda} \Gamma\left(1 + \frac{1}{a}\right) \quad (2-10)$$

Where λ is the scale parameter, a is the shape parameter, and $\Gamma(x)$ is the gamma function. When a is greater than one the failure rate of the components is increasing with time, the larger the value of the shape parameter, a , the steeper the increase in the failure rate of the components; when $a = 1$ you get the exponential distribution which is actually a special case of the Weibull distribution. The Weibull distribution is a generalization of the exponential distribution that is appropriate for modeling lifetimes having constant, strictly increasing, and strictly decreasing hazard functions [Leemis, 1995]. The exponential distribution has a constant failure rate often making it too restrictive for the use in modeling failures in electronic components. The Weibull distribution is often used to model failure rates in electronic components, the exponential distribution is “memoryless” and is a good distribution for modeling something with a constant/steady hazard rate, and lastly items that might show wear, such as mechanical items, often degrade over time so a distribution with an increasing hazard function should be chosen.

Note that the Mean Time Between Failures, MTBF, is used to describe the performance of “repairable systems” and in general is not the same as the MTTF. Also, please note that the median time to failure is the time at which 50% of the population will survive, $R(t_{0.5})=0.5$, often denoted by T_{50} . A list of useful statistical information is shown in Table 2-1.

Table 2-1 Information on various parametric distributions

	Exponential Distribution	Lognormal Distribution	Weibull Distribution
Parameter	λ : failure _ rate	μ : log mean σ : shape	α : scale β : shape
Probability Density Function	$f(t) = \lambda \exp(-\lambda t)$	$f(t) = \frac{1}{\sigma t \sqrt{2\pi}} \exp\left[-\left(\frac{1}{2\sigma^2}\right)(\log(t) - \mu)^2\right]$	$f(t) = \frac{\beta}{t} \left(\frac{t}{\alpha}\right)^{\beta} \exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right]$
Reliability Function	$R(t) = \exp(-\lambda t)$	$R(t) = 1 - \Phi\left[\frac{\log(t) - \mu}{\sigma}\right]$	$R(t) = \exp\left[-\left(\frac{t}{\alpha}\right)^{\beta}\right]$
Mean Time to Failure (MTTF)	$MTTF = 1 / \lambda$	$MTTF = \exp\left(\mu + \frac{\sigma^2}{2}\right)$	$MTTF = \alpha \cdot \Gamma\left(1 + \frac{1}{\beta}\right)$
Hazard Rate	$h(t) = \lambda$	$h(t) = \frac{\Phi\left(\frac{\ln t - \mu}{\sigma}\right)}{t \sigma R(t)}$	$h(t) = \frac{\beta}{\alpha} \left(\frac{t}{\alpha}\right)^{\beta-1}$
Scale (Minitab)	$Scale_{minitab} = 1/\lambda$	$Scale_{minitab} = \sigma$	$Scale_{minitab} = \alpha$
Shape (Minitab)	N/A	N/A	$Shape_{minitab} = \beta$

The characteristic life percentile, $F(t)=0.632$, corresponds to when t equals the scale parameter for the Weibull distribution [Tobias 1986]. This is another reliability metric presented in many publications in addition to the MTTF or the MTBF. The characteristic life of the Weibull distribution is a special case when the failure time is equal to the scale parameter; this corresponds to the time when the cumulative failure distribution is at ~63.2%. Typically the failure data from electronic components will fit one of the above listed parametric distributions. The plot of the reliability function versus time for the Weibull distribution for all values of the shape parameter will intersect at this point. As mentioned earlier, when the shape parameter is one the Weibull distribution becomes the exponential distribution; the exponential distribution is good for modeling components with a constant failure rate. This also means that a component at

time $t + \Delta t$ is as likely to fail as a component at t . When the shape parameter is equal to 2, another special case of the Weibull distribution emerges, known as the Rayleigh distribution [Ohring, 1998]. Rayleigh distributions are not normally used to describe the reliability of electronic components; however, this distribution function is often useful in modeling failures with an increasing hazard functions [Ohring, 1998].

Lognormal and Weibull distributions are often both very good at modeling failure times for electronic components; however, subtle differences in failure rates and failure mechanisms might lead to one versus the other. For example, lognormal distributions tend to apply when gradual degradation occurs over time because of diffusion effects, corrosion, and chemical reactions (bi-polar and MOS transistor failures or LED failures are good examples of failures that are modeled well with a lognormal distribution). Weibull distributions appear to be applicable in cases where a weak link propagates to failure; examples would be: dielectric breakdown, capacitor failures, and failures in solder [Ohring, 1998].

2.4.2.2 General Procedure for Statistical Evaluation of Failure Times

To determine the reliability performance of several components the statistics based methodology requires that several test vehicles with critical structures are assembled and tested in accelerated life testing. All failures are analyzed to determine the root cause of failure. The next step is to fit the failure data to a parametric lifetime distribution (Weibull, Normal, Exponential, etc.). In MinitabTM the Maximum Likelihood Estimation is a general method for estimating the statistical parameters. A

probability plot is generally a good method for determining which of the parametric distributions is the best fit to the failure data. In addition, MinitabTM will output an Anderson-Darling statistic which is a goodness-of-fit statistic to help compare which distribution fits the data most closely. The Anderson-Darling statistic is a measure of how far the plotted points fall from the fitted line in a probability plot. The statistic is a weighted squared distance from the plotted points to the fitted line with larger weights in the tails of the distribution [MinitabTM, 2000]. The distribution that gives the lowest value of the statistic generally is the distribution that best fits the data points that were entered into MinitabTM. It should be noted that several distributions might have similar A-D statistics and therefore it is up to the engineer to use other methods to assess which of the lifetime distributions best describes the data, special attention should be paid to which distributions have been good fits in past experiments for the same failure mechanisms.

The central building block in reliability prediction is the fundamental knowledge of material behavior at the stress levels that the package will experience while in the use environment. For the purposes of illustration a diffusion mechanism is chosen to illustrate the method by which acceleration factors can be used to determine what the field failure rate is for an electronic component based on some standard accelerated life testing results obtained in a lab environment at elevated stress levels. First the Arrhenius model is used to discuss a diffusion mechanism, and second, For example, if there is a chemical or physical failure mechanism that can be accelerated by temperature as the ‘stress’ the Arrhenius Model is often employed. The diffusion coefficient for thermally activated solid-state diffusion can be expressed with an Arrhenius relationship (Shewman 1963).

$$D = D_o e^{-(Q/RT)} \quad (2-11)$$

Where:

D = the diffusion coefficient at temperature T

D_o = the frequency and entropy coefficient

Q = the enthalpy of atomic motion

R = the gas constant, 8.3143 joules per mole, degree Kelvin

At a constant diffusion length, identical solutions for the diffusion equation occur [Shewman 1963].

$$Dt = C \quad (2-12)$$

The time to fail corresponding to accumulation of a critical void volume at a given temperature, T is given by:

$$t_f = Ae^{(Q/RT)} \quad (2-13)$$

Comparing the time to fail at one temperature with the failure time at another temperature yields

$$t_{f_1} = t_{f_2} \exp \left[\frac{Q}{R} \left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right] \quad (2-14)$$

The acceleration factor can be written as follows:

$$AF = \frac{t_{f_1}}{t_{f_2}} = \exp \left[\frac{Q}{R} \left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right] \quad (2-15)$$

It should be noted that the expression above can be used in a similar manor for other thermally activated failure mechanisms such as growth of oxide scales and corrosions films.

In general terms, the time to failure listed in the above expression can be taken as the characteristic lifetime of the Weibull parametric failure distribution. If the temperature dependence of the scale parameter is known via experimental analysis the following relation results:

$$\lambda_f = Ae^{(Q/RT)} \quad (2-16)$$

Similarly, a power law relationship could be used for failure mechanisms that follow a general log base e relationship. These calculations are all conducted via Minitab™ analysis using the Accelerated Life Testing option. The acceleration variable for the example of diffusion above would be temperature and the relationship is Arrhenius. An assumed distribution can also be defined for the analysis. The use of Minitab™ statistical analysis software makes the extrapolation of failure data from the lab environment very easy if there is failure data obtained at more than one temperature point. Notice that the data in the figure shows equal slopes for all of the test conditions. Minitab™ statistical analysis software offers a formal test to determine if the slopes are equal, the following menu path can be used: Stat→Reliability/Survival→Parametric Distribution Analysis→(a window will appear) select ‘test’→select the appropriate test→click OK. The acceleration factor is used to extrapolate the lab data to a field use

environment failure curve. Figure 2-4 shows a probability plot of failure data from three test conditions to the field use condition. The use condition line is on the right most part of the graph.

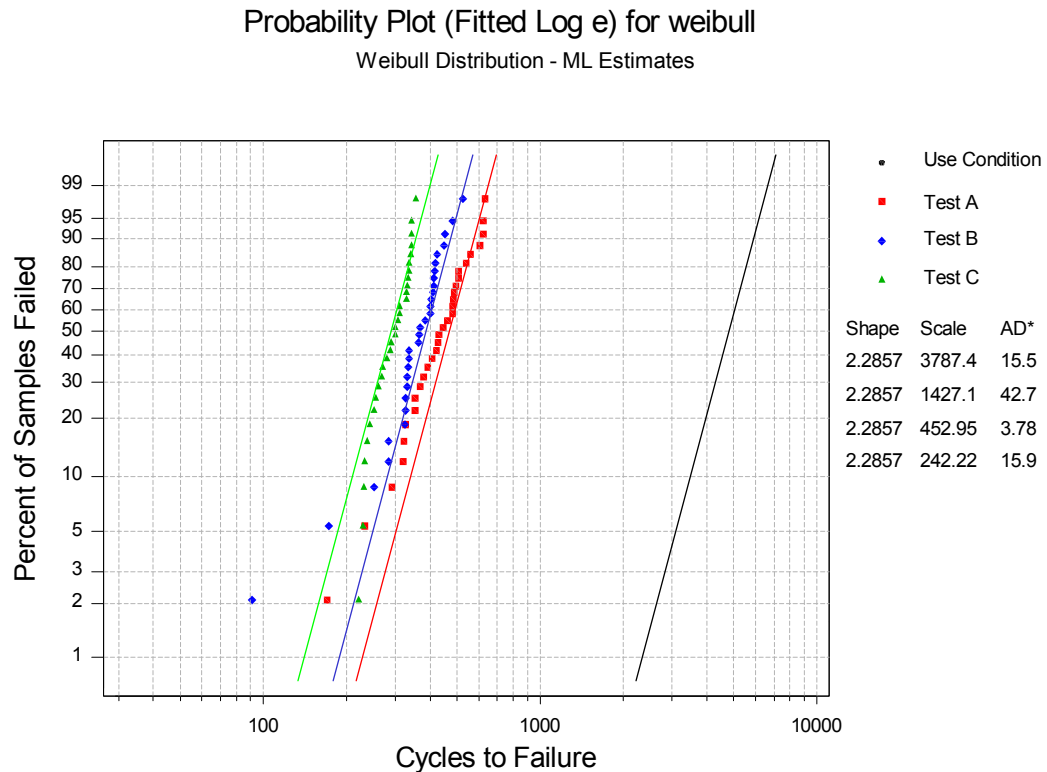


Figure 2-4 Probability Plot showing the Extrapolation from Test Conditions to Use Conditions

2.4.3 Reliability Models

2.4.3.1 Fatigue of Solder

Fatigue of solder joints in electronic assemblies is believed to play a role in 90% of all structural and electrical failures [Tummala 2001]. There are two general

classifications of fatigue, stress-based fatigue and strain-based fatigue [Dowling]. These fatigue equations predict the initiation of cracks; the propagation of cracks can be analyzed with the Paris-Law. In electronic packaging, it is assumed that the initiation of the crack is synonymous with the end of component life. The stress-based approach generally applies to high cycle fatigue for materials that are still within the elastic regime. The strain-based approach is comprised of two terms; one of which is largely for elastic deformation and high cycle fatigue, and the second term allows for inelastic deformation of the material and is generally used for low cycle fatigue. For fatigue of solder joints, the Coffin-Manson equation can be written as a function of the inelastic shear strain range, $\Delta\gamma$, given by [Manson & Coffin 1965, 1954]:

$$N_f = \frac{1}{2} \left(\frac{\Delta\gamma}{2\varepsilon'_f} \right)^{1/c} \quad (2-17)$$

Where N_f is the cycles to fatigue failure. ε'_f is the fatigue ductility coefficient and c is the fatigue ductility exponent. These represent the fatigue characteristics of a given material. Other strain based fatigue equations have been proposed by several authors. Solomon developed a similar equation that was based on plastic shear strain range for Pb-Sn solders using simple shear experiments [Soloman, 1986].

$$N_f = \left(\frac{\theta}{\Delta\gamma_p} \right)^{1/\alpha} \quad (2-18)$$

Soloman's model was for 60/40 solder, and fatigue was defined as the number of cycles to halve the load range required to produce plastic strain. The constants for this model were developed for solder under simple shear testing conditions. This equation is based

on the plastic shear strain range For the temperature range of -50°C to 125°C the constants θ and α are 1.14 and 0.51 respectively. Please note that N_f is cycles to halve the load range, $\Delta\gamma_p$ was measured as a percentage, γ_p was measured in *in/in* .

Engelmaier modified the constants of Soloman's equation to account for cyclic frequency [Engelmaier 1983]. The Engelmaier model appears to be the precursor to the model found in the IPC-SM-785 spec. Engelmaier develops an equation for the cyclic shear strain range in the corner solder joint, neglecting both warpage and transient strains and assuming an ideal joint geometry giving a uniform strain distribution as well as no brittle regions in the joint due to solder intermetallics or weak metallization.

$$\Delta\gamma = \frac{L\Delta(\alpha\Delta T)_{ss} \times 10^{-4}}{\sqrt{2}h} \quad (2-19)$$

$$N_f = \frac{1}{2} \left(\frac{\Delta\gamma_{\max_range}}{2\varepsilon_f'} \right)^{\frac{1}{c}} \quad (2-20)$$

where:

$\Delta\gamma$ = cyclic shear strain range in the corner joint, %

h = height of the solder joint

$\Delta(\alpha\Delta T)_{ss} = (\alpha_c - \alpha_s) \cdot (T_c - T_o)$, for temperature cycle

α_c, α_s coefficients of linear thermal expansion for a ceramic chip carrier and substrate, respectively

T_c temperature of the ceramic ship carrier

T_o power off, steady-state temperature

L = length of ceramic chip carrier

$$c = -0.442 - 6 \times 10^{-4} T_s + 1.74 \times 10^{-2} \ln(1 + f)$$

f = is the cyclic frequency in cycles per day

N_f = mean cycles to failure

ε_f' = the fatigue ductility coefficient

T_s is the mean cyclic solder joint temperature, °C

$$2\varepsilon_f' \approx 0.65 \text{ [Engelmaier 1983]}$$

A modified version of the Engelmaier equation is found in the IPC-SM-785 spec that also accounts for CTE mismatch and assumes a proposed Weibull failure distribution. However, the specification warns that the provided equation should not be used in the transition region between -20°C and 20°C. In general, this specification gives great background information on reliability of solder interconnects. The model presented in this specification appears to be a modified version of the model developed by Engelmaier in the 80s. This model incorporates the statistical distribution of failures that are in large part represented by the Weibull distribution. The fatigue life of solder joints, $N_f(x\%)$, at a given acceptable failure probability, x , can be predicted for both isothermal-mechanical and thermal cycling by the following equation. Note, the below equation is

for stiff leaded joints where the stresses in the solder joints exceed the solder yield strength.

$$N_f(x\%) = \frac{1}{2} \left[\frac{2e'_f h}{FL_D \Delta \alpha \Delta T_e} \right] - \frac{1}{c} \left[\frac{\ln(1 - 0.01x)}{\ln(0.5)} \right]^{1/\beta} \quad (2-21)$$

There is also an equation given for a compliant leaded solder attachment:

$$N_f(x\%) = \frac{1}{2} \left[\frac{2e'_f (200 \text{ psi}) Ah}{FK_D (L_D \Delta \alpha \Delta T_e)^2} \right] - \frac{1}{c} \left[\frac{\ln(1 - 0.01x)}{\ln(0.5)} \right]^{1/\beta} \quad (2-22)$$

Where c is defined as:

$$c = -0.442 - 6 \times 10^{-4} T_{sj} + 1.74 \times 10^{-2} \ln \left(1 + \frac{360}{t_D} \right) \quad (2-23)$$

The remainder of the variables are defined in Table 2-2:

Table 2-2 Variables for IPC-SM-785 Reliability Specification

Variable	Description
A	effective minimum load bearing solder joint area (~2/3 solder wetted lead area projected to the solder pad)
c	fatigue ductility exponent defined above
F	empirical "non-ideal" factor indicative of the deviations of real solder joints from idealizing assumptions and accounting for the secondary and frequency intractable effects such as cyclic warpage, cyclic transients, non-ideal solder joint reliability, brittle intermetallic compounds, Pb-rich boundary layers, and solder/bonded-material expansion differences, as well as inaccuracies and uncertainties in the parameters in the equations listed above. $1.5 > F > 1.0$ for column like leaded attachments, $1.2 > F > 0.7$ for leadless solder attachments.
h	solder joint height
K_D	"diagonal" flexural stiffness of unconstrained, not soldered, component lead, determined by strain energy methods, or finite element analysis
$2L_D$	maximum distance between component solder joints measured from component solder joint pad centers
N	number of operating cycles during product life
$N_f(x\%)$	number of operating cycles to x% failure probability
T_c, T_s	steady state operating temperature for component, substrate during high temperature dwell
$T_{c.o.}, T_{s.o.}$	steady state operating temperature for component, substrate during low temperature dwell, for non-operational (power off) half-cycles these equal each other
T_{sj}	$1/4*(T_c + T_s + T_{c.o.} + T_{s.o.})$, mean cyclic solder joint temperature
t_D	half cycle dwell time in minutes, average time available for stress relaxation at the high and the low temperatures
x	acceptable cumulative failure probability for the component under consideration after N cycles, %.
α_c, α_s	coefficient of thermal expansion for the component, substrate
β	Weibull shape parameter, slope of the weibull probability plot
ΔD	potential cyclic fatigue damage at complete stress relaxation
ΔT_C	cyclic temperature swing for component, $T_c - T_{c.o.}$
ΔT_e	absolute value of $(\alpha_s \Delta T_s - \alpha_c \Delta T_C) / \Delta \alpha$, equivalent cycling temperature swing, accounting for component power dissipation effects as well as component external temperature variations ($\Delta \alpha$ is not equal to 0)
ΔT_S	cyclic temperature swing for substrate, $T_s - T_{s.o.}$
$\Delta \alpha$	absolute value of $(\alpha_c - \alpha_s)$, absolute difference in coefficients of thermal expansion of component and substrate, CTE-mismatch
e_f'	fatigue ductility coefficient, $2e_f' \sim 0.65$ for near eutectic tin-lead solder

Knecht and Fox proposed an equation that relates fatigue life with a creep strain component due to matrix creep only (creep shear strain range), ignoring plastic deformation [Knecht & Fox 1991].

$$N_f = \frac{C}{\Delta\gamma_{mc}} \quad (2-24)$$

The mc subscript on the gamma term stands for matrix creep. The constant, C , for 60/40 & 63/37 solder are 8.9 and 1.7 respectively. It should be noted that to use of this equation in conjunction with finite element modeling the model must be able to separate the inelastic effects into creep strain (time dependant inelastic strain) and plastic strain (time independent inelastic strain). Please note that N_f is cycles to failure, $\Delta\gamma_{mc}$ was measured as a percentage.

There are also many equations proposed for specific types of electronic packages, many of these are empirical fits to experimental data. B.Z. Hong developed a relation for ceramic BGAs that related the plastic shear strain range to the average fatigue life of the solder joints [Hong 1997]. A nonlinear finite element model is presented for analyzing the cyclic and thermal fatigue loading and for viscoplastic damage characterization of the Pb-Sn solder joints in a CBGA surface mount package. Hong's approach uses a modified Coffin-Manson equation with a saturated equivalent inelastic strain range as determined by FEM. Hong mentions that the time-dependent (creep induced) damage mechanism is found to be more pronounced than the time-independent (plastic deformation) mechanism. Hong's approach uses a distance from neutral point concept to calculate the shear strain purely due to the global mismatch of thermal expansions between the two

components adjacent to the solder joint. A thermal load from 0°C to 100°C was used in the development of this model. Hong refers to a ratcheting response of the solder. He also shows the stress strain curves for solder at different temperatures. Where $B = 1.2928$ and $C = -1.96$. Note, that he used the same alpha and theta that Solomon determined [Soloman, 1986].

$$N_f = B(\Delta\varepsilon_{eq}^{in})^c \quad (2-25)$$

Hong's equation is a good example of an empirical fit to experimental data. This equation is limited in its use, simply because it does not address the physics behind the failures. For example, if there are voids in the underfill that increase the strain experienced by the solder joints then the amount of cycles to failure will change, however this type of equation will not capture the affect of a process induced defect such as voiding in solder joints.

Lau et. al. published equations for leadless and leaded solder joints relating fatigue life to the total shear strain range and the maximum equivalent plastic strain, respectively [Lau, 1997]. The failure criteria for the leadless solder joints are based upon the total strain range determined by the given temperature cycle profile and treating solder as elastic and viscoplastic. Thermal cycling test data by Sherry and Hall were used to correlate the predicted strain range. This is a Coffin-Manson-type of relation that exists between the total strain range and the thermal fatigue life. It should be noted that all the eleven tests conducted by Sherry and Hall had different temperature extremes, hold times, and ramp rates [Sherry *et al.*, 1986]. This model is for 63/37 solder joints.

$$N_f = 3.013(\Delta\gamma_{max_range})^{-0.924}, \text{ in cycles} \quad (2-26)$$

In Lau's analysis for leaded solder joints the approach that was used was based on a modified version of the method used by Kitano et al. The leads are treated as simple beams, and the solder is modeled as a temperature-dependant elastic-plastic material. The time dependant behavior of the solder is incorporated through a frequency-dependant parameter in the constitutive equation. Creep and stress relaxation of the solder are not considered in this model. The equivalent strain, a collective measure of the normal and shear strain, was determined along the lead foot length, and the maximum value was used to calculate fatigue life of the solder, $\gamma_{\max_equivalent_plastic}$.

$$N_f = 2.277 \times 10^{-3} (\gamma_{\max_equivalent_plastic})^{-2.61} \quad (2-27)$$

Many of these equations are used in conjunction with finite element modeling to 'predict' fatigue failure. A popular method published by Darveaux determines the strain energy density accumulated in solder per thermal cycle and calculates the number of cycles to crack initiation, and the number of cycles to propagate the crack through the solder joint [Darveaux 1997]. The paper by Darveaux focuses on the aspects of the finite element analysis that affect fatigue life prediction, such as the time and temperature dependent material properties, element size, singularities, load step size and interpretation of the results. An iterative process was used to determine the Anand constants that gave approximately the same results as the Darveaux model. The model uses FEA to calculate the viscoplastic strain energy density accumulated per cycle during thermal or power cycling. The strain energy density is then used with crack growth data to calculate the number of cycles to initiate cracks and the number of cycles to propagate cracks through

the thickness of the joint. The constitutive equations used in Darveaux's model used steady state creep, transient creep at constant stress and temp and then took the time derivative of the transient creep equation. Resulting in an instantaneous creep rate and a steady state creep rate. Then, at high stresses the author suggests, there is also a time-independent plastic strain component of deformation. This plastic strain is added to the creep strain to form the total inelastic creep strain. However, these equations are not available in ANSYSTM, so through an iterative process Darveaux compared the results of his model to those generated by Anand's model (which is comprised of a flow equation and three evolution equations). ANSYSTM provides viscoplastic elements as a standard option, however this element type utilizes Anand's constitutive model [Anand, 1985]. Darveaux determines the constants for Anand's model, this allows the FEM programmer to use the constitute equations that accurately define the behavior of solder without actually having to hard-code them into the FEM code. Instead, you use the Anand's constants that are given in the paper. These constants are for 62Sn36Pb2Ag solder. The author warns that the relative predictive life predictions are more accurate than the absolute life predictions.

$$\text{Crack initiation: } N_o = C_3 \Delta W_{ave} C_4 \quad (2-28)$$

$$\text{Crack Growth: } \frac{da}{dN} = C_5 \Delta W_{ave} C_6 \quad (2-29)$$

$$\text{Characteristic Life: } \alpha = N_o + \frac{a}{da/dN} \quad (2-30)$$

Table 2-3 Values for Darveaux's Model [Darveaux, 1997]

Element thickness along Interface (mm)	C_3 (cycles/MPa ^{C₄})	C_4	C_5 (mm/(cycle*MPa ^{C₆}))	C_6
0.00762	26.97	-1.39	1.2719*10 ⁻³	1.14
0.00762	31.571	-1.42	1.0694*10 ⁻³	1.13
0.01524	20.685	-1.44	1.4922*10 ⁻³	1.15
0.03302	12.633	-1.46	2.1529*10 ⁻³	1.15
0.0508	9.6725	-1.45	2.6241*10 ⁻³	1.12

ANSYS 5.2, a commercially available finite element package, uses a constitutive model by Anand for its viscoplastic element type. The Anand model incorporates a flow equation and three evolution equations in an attempt to unify the time dependant and time independent inelastic deformation of a material into a single set of equations [Anand, 1985]. Using an iterative process Darveaux determined the Anand constants that gave approximately the same solution as the Darveaux model for solder, allowing one to use the Darveaux model without modifying the source code in ANSYS. This is relevant because it allows anyone to incorporate the Darveaux's constants for the inelastic behavior of solder into ANSYS easily, in addition this model combines the creep strain and plastic strain which allows for faster simulation run times.

Cheng et. al . used Anand's model for finite element modeling of Pb-rich solder alloys in a flip chip assembly and thin quad flat pack [Cheng, 2000]. The flip chip used in Cheng's analysis had copper bumps.

Amagai developed a model for CSP solder joint reliability that incorporated some of the physical attributes of the component level package. A viscoplastic constitutive model was used to analyze the thermally induced plastic and creep deformation and low cycle fatigue behavior of the solder joints in Chip Scale Packages mounted on Printed

Circuit Boards. Anand's model was used in FEM simulation along with the results of several reliability tests to determine an equation that relates the total strain range as a function of the number of cycles to a 50% cumulative failure in 0.6mm diameter solder balls.

$$N_f(50\%) = \left(\frac{\Delta \varepsilon}{33.83} \right)^{1.93}, \text{ in cycles.} \quad (2-31)$$

This design and model was then simplified (generalized) to accommodate other CSP package sizes. The 2D plane strain FEM viscoplastic model was executed for a flexible substrate CSP with a variety of chip sizes and package sizes. The temperature cycling was from -40°C to 125°C with a 1-minute ramp and a 9-minute dwell resulting in a total of 3 cycles per hour.

$$F = \frac{100C^2}{SP^2} \quad (2-32)$$

Where

C is the chip size in mm

P is the package size in mm

S is the number of solder balls

$$N_f(50\%) = \left(\frac{100C^2}{14402SP^2} \right)^{-0.62112} \quad (2-33)$$

Which gives this following general form where A and B are determined by material property and package dimension. A shortcoming with this model is that the methods by which A and B are determined is not well described in the paper [Amagai, 1999].

$$N_f(50\%) = \left(\frac{100C^2}{BSP^2} \right)^{-A} \quad (2-34)$$

2.5 Basic Discussion of Deformation Terms

This section will provide a short discussion on elastic and plastic deformation to provide some description of terms that are used throughout this thesis. Stress is the amount of force per unit area, and strain is the amount of extension of a sample divided by the initial length. Macroscopically speaking, materials react to an applied stress in two ways (1) elastically and (2) plastically. Elastic behavior is not permanent and will recover if the applied load is removed, plastic behavior describes the condition when the stress is removed and the strain does not return back to zero. The point where the behavior changes from elastic to plastic is the yield point.

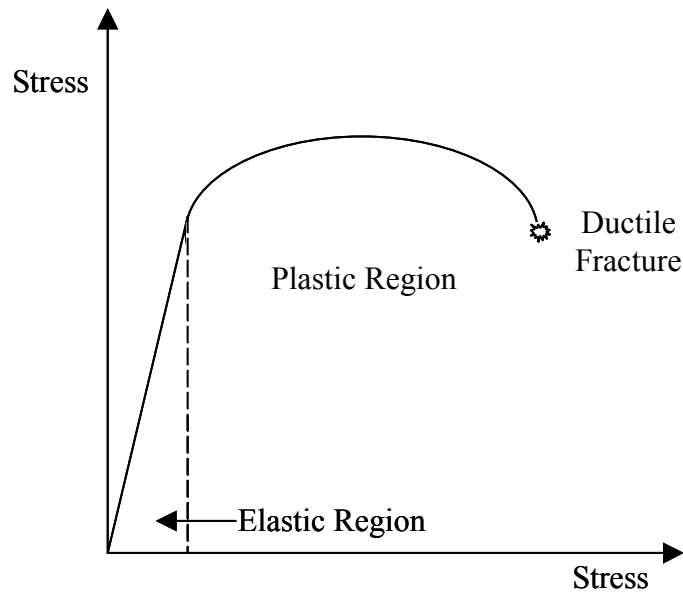


Figure 2-5 Stress/Strain Diagram

For most materials, the plastic deformation depends not only upon the maximum value of stress that is achieved, but also the time that is elapsed before the stress is removed. The stress dependant part of the plastic deformation is referred to as *slip* and the time dependant part (which is also influenced by temperature) is referred to as *creep* [Beer & Johnston, 1992].

Creep behavior, or time-dependant plastic behavior, can be subdivided into three main categories: primary, secondary, and tertiary creep. A general drawing of creep behavior is shown in the figure below.

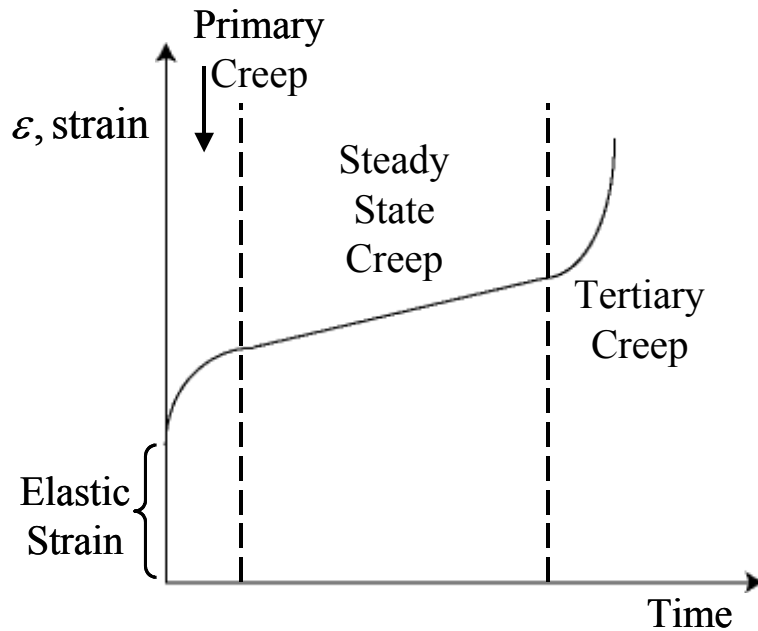


Figure 2-6 Primary, Secondary, and Tertiary Creep [Dowling, 1999]

Primary creep or transient creep can occur relatively rapidly with a high initial strain rate, $\dot{\epsilon} = d\epsilon/dt$, followed by a reduction in $\dot{\epsilon}$ until it becomes constant, at this point primary creep ends and secondary creep begins [Dowling, 1999]. Secondary creep is known as steady state creep. Finally, the creep rate increases again until the point of creep rupture, or failure.

To discuss the creep phenomena it is helpful to look at a one-dimensional defect in a crystal lattice structure. Please note that a grain boundary is a two-dimensional defect, which is largely made up of vacancies. A simple way to show a one-dimensional defect is to show a crystal lattice structure with an extra $\frac{1}{2}$ plane of atoms inserted into it as shown in the figure below.

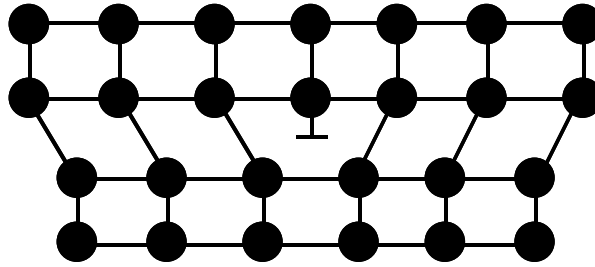


Figure 2-7 Atomic scale image of a line dislocation in a crystal lattice

In the figure above there is a $\frac{1}{2}$ plane of atoms missing; this plane goes in and out of the paper. In the center of the drawing you will find a dislocation line. When a material plastically deforms it is this dislocation line that moves through the material under an applied stress. When a dislocation moves due to an applied stress the process is called thermally activated climb. The climb mechanism requires a whole line of atoms (into and out of the paper when referring to the figure above) to diffuse away from the dislocation, resulting in movement of the dislocation upward (a movement of the dislocation laterally would be the glide mechanism). *Dislocation creep* is only one of the physical mechanisms; other mechanisms are *diffusional flow* and *grain boundary sliding*. A general equation for the steady-state creep rate in *crystalline* materials is

$$\dot{\epsilon} = \frac{A_2 \sigma^m}{d^q T} e^{\frac{-Q}{RT}} \quad (2-35)$$

Where:

$\dot{\epsilon}$ = the strain rate

σ = stress

d = average grain diameter

T = absolute temperature

A_2, m, q, Q = are material dependant and vary based on creep mechanism that is acting

The creep exponents for various physical creep mechanisms are shown in the table below.

Table 2-4 Creep Exponents for various Physical Mechanisms [Dowling, 1999]

Name of Mechanism	m	q	Description
Diffusional flow (Nabarro-Herring Creep)	1	2	Vacancy diffusion through the crystal lattice
Diffusional flow (Coble Creep)	1	3	Vacancy diffusion along grain boundaries
Grain Boundary Sliding	2	2 or 3	Sliding accommodated by vacancy diffusion through crystal lattice ($q=2$) or along grain boundaries ($q=3$)
Dislocation creep (power law creep)	3 to 8	0	Dislocation motion, with climb over microstructural obstacles

3 SCOPE AND OBJECTIVES

Environmental stress tests, or accelerated life tests, apply stresses to electronic packages that exceed the stress levels experienced in the field. In theory, these elevated stress levels are used to generate the same failure mechanisms that are seen in the field, only at an accelerated rate. The methods of assessing reliability of electronic packages can be classified into two categories: a statistical failure based approach and a physics of failure based approach. This research uses a statistical based methodology to identify the critical factors in reliability performance of a flip chip on board component level assembly and a physics of failure based approach to develop a low cycle strain based fatigue equation for flip chip component level assemblies. The critical factors in determining reliability performance were established via experimental investigation and their influence quantified via regression analysis. This methodology differs from other strain based fatigue approaches because it is not an empirical fit to experimental data; it utilizes regression analysis and least squares to obtain correction factors, or correction functions, and constants for a strain based fatigue equation, where the total inelastic strain is determined analytically. The end product is a general flip chip on board equation rather than one that is specific to a certain test vehicle or material set.

Specific objectives of the work included:

1. To study the effects of substrate metallization on the reliability performance of flip chip on organic board assemblies.
2. To study the effects of various underfill materials on the reliability performance of flip chip on board assemblies.

3. To analytically determine the total inelastic strain in a solder joint as a result of temperature cycle.
4. To develop a 2D-finite element model of a flip chip on board assembly. This will serve as a control for the prediction of cycles to failure of a flip chip on board assembly. In addition, it will be used to provide information on the effects of changing material properties and geometries on the predicted number of cycles to fatigue failure.
5. To generate a comprehensive strain based fatigue equation that includes correction factors for substrate bond pad metallization, underfill material properties, and solder joint shape.
6. Assemble and test various assemblies in thermal cycle and thermal shock to obtain a set of failure data.
7. Utilize statistical regression techniques to determine appropriate correction factors, or correction functions, for a strain based fatigue equation.
8. To determine the root cause of failure in assemblies by utilizing x-ray imaging, c-mode scanning acoustic microscopy, cross section analysis, scanning electron microscopy, and electron discharge spectroscopy.
9. To study the intermetallic growth and shear strength degradation of flip chip solder bumps after 400 hours of thermal aging at 125°C; for Cu/Ni/Au and Cu/OSP surface finishes bonded to eutectic Sn 63/Pb 37 solder bumps.
10. To quantify the effects of thermal aging of underfill materials on the material properties of the underfill material, Modulus, glass transition temperature, and

coefficient of thermal expansion will be monitored post-reflow/pre-thermal age and post-thermal age.

4 EXPERIMENTAL DATA COLLECTION & FINITE ELEMENT MODELING

4.1 Assembly

The primary goal of this thesis research was to develop a reliability modeling methodology for predicting the reliability performance of a flip chip on board component level assembly. To accomplish this goal, it was first necessary to generate a large amount of failure data for a flip chip on board component level package structure. Over 3000 test vehicles were assembled using an assembly process developed by Lazarakis and Baldwin [Lazarakis, 2003]. The general outline of the assembly process will be described in this section for the purposes of completeness. Detailed process development information can be found in Lazarakis' thesis [Lazarakis, 2003].

4.1.1 Test Vehicles

The test vehicles used throughout the experimental portion of this project were assembled with 5 flip chip test die, 9 circuit boards, and three no-flow underfill materials. The test chips used in the experimentation were daisy chain test die provided by Flip Chip Technologies LLC. The daisy chain structure on the die in conjunction with the copper traces embedded in the circuit boards allowed for easy 2 point resistance measurements to verify the integrity of the interconnect structure after the components had been stressed in accelerated life testing. The metallization on the circuit boards was e(1) Copper/Electroless Nickel/Immersion Gold (these will be referred to as the Ni/Au

boards throughout this thesis), or (2) Copper/Organic Solderability Preservative (OSP). The thickness of the substrates varied from 0.7874mm to 1.46mm thick.

4.1.1.1 PB8 2x2 Test Vehicle

The perimeter bumped PB8-2x2 flip chip was mounted on a circuit board that had 12 individual die sites. The PB8-2x2 measured 5.08mm x 5.08mm (0.2 inches x 0.2 inches) in overall size, a total I/O count of 88 63Sn/37Pb flip chip bumps, and a bump to bump pitch of 203 microns. A general schematic of the PB8 2x2 test die is shown in Figure 4-5. The bump diameter was 120 microns and the height of each individual bump was 98 microns, after collapse the standoff height for this flip chip was found to be approximately 71 microns. The substrate had a glass transition temperature of 120 °C and a thickness of 0.7874 mm. There were two bond pad metallizations for this substrate: Cu/Ni/Au and Cu/OSP. The Cu/Ni/Au metallization was 0.043mm of copper, 2.73 microns of electroless Nickel (measurements in Figure 4-8), and an immersion gold layer which was 0.084 microns thick on average (measurements in Figure 4-7). The second metallization, Cu/OSP, consisted of 0.045 mm of copper and a layer of organic solderability preservative that ranged in thickness from 0.05 to 0.13 microns. The substrate bond pads were hybrid in nature with two sides that were solder mask defined, SMD, and two sides that were non-solder mask defined, NSMD. The overall shape of the bond pads was a rectangle (Figure 4-6).

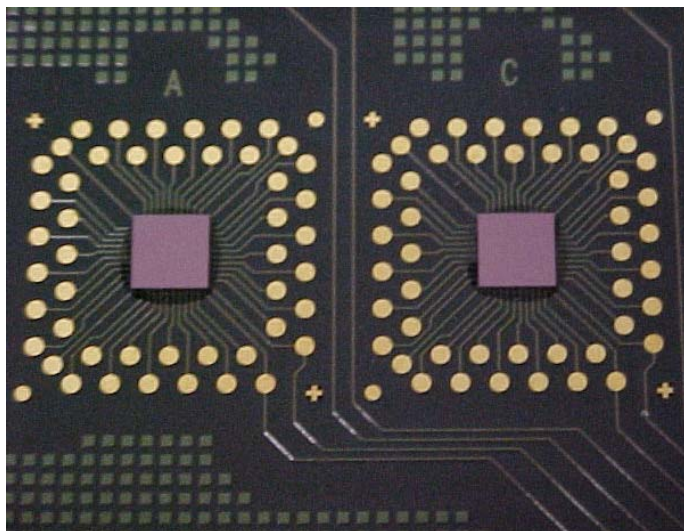


Figure 4-1 PB8 2x2 Picture of Assembled Test Vehicle

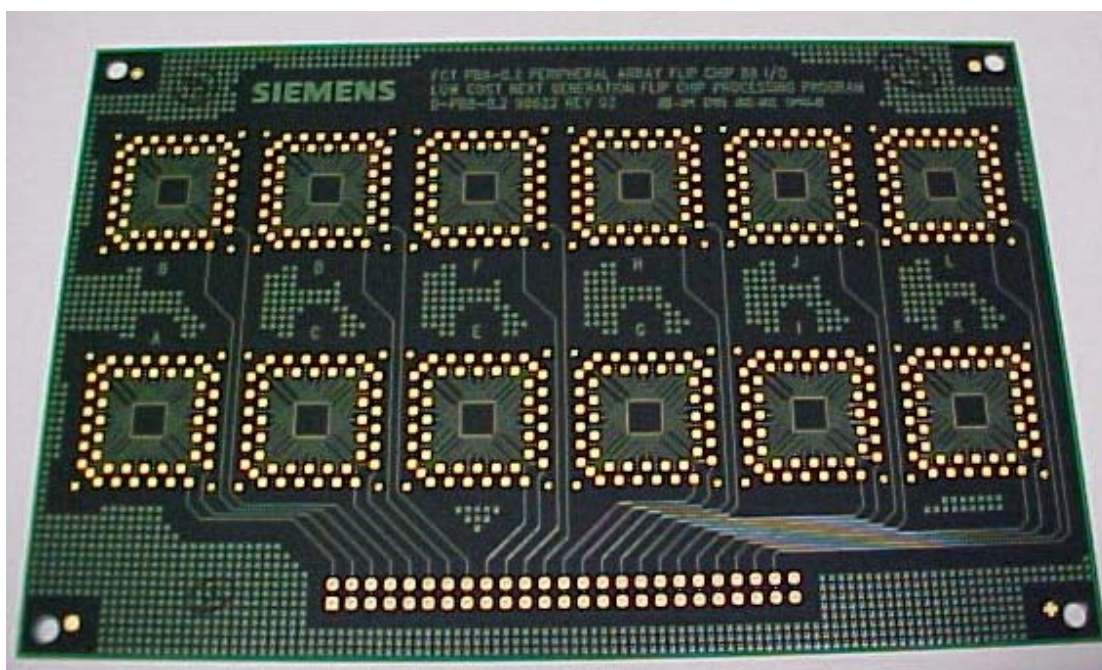


Figure 4-2 Substrate for PB8 2x2 Test Vehicle

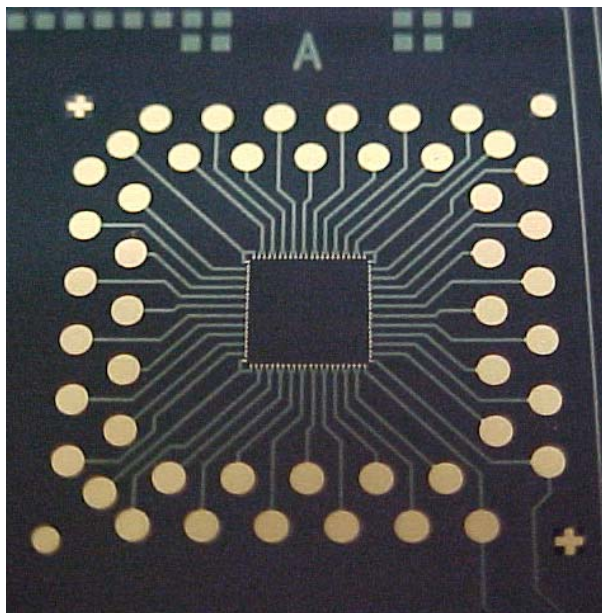


Figure 4-3 Close-Up View of a PB8 Die site on PCB

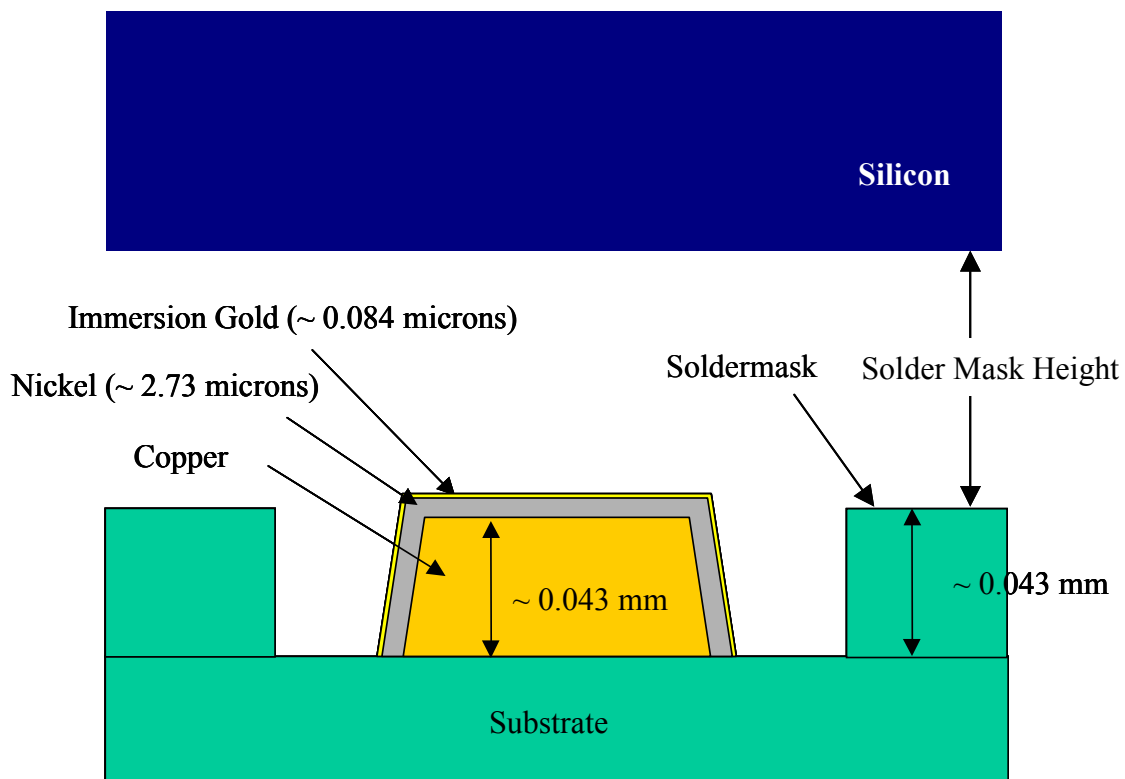


Figure 4-4 Schematic of Metallization of the Substrate Bond Pads

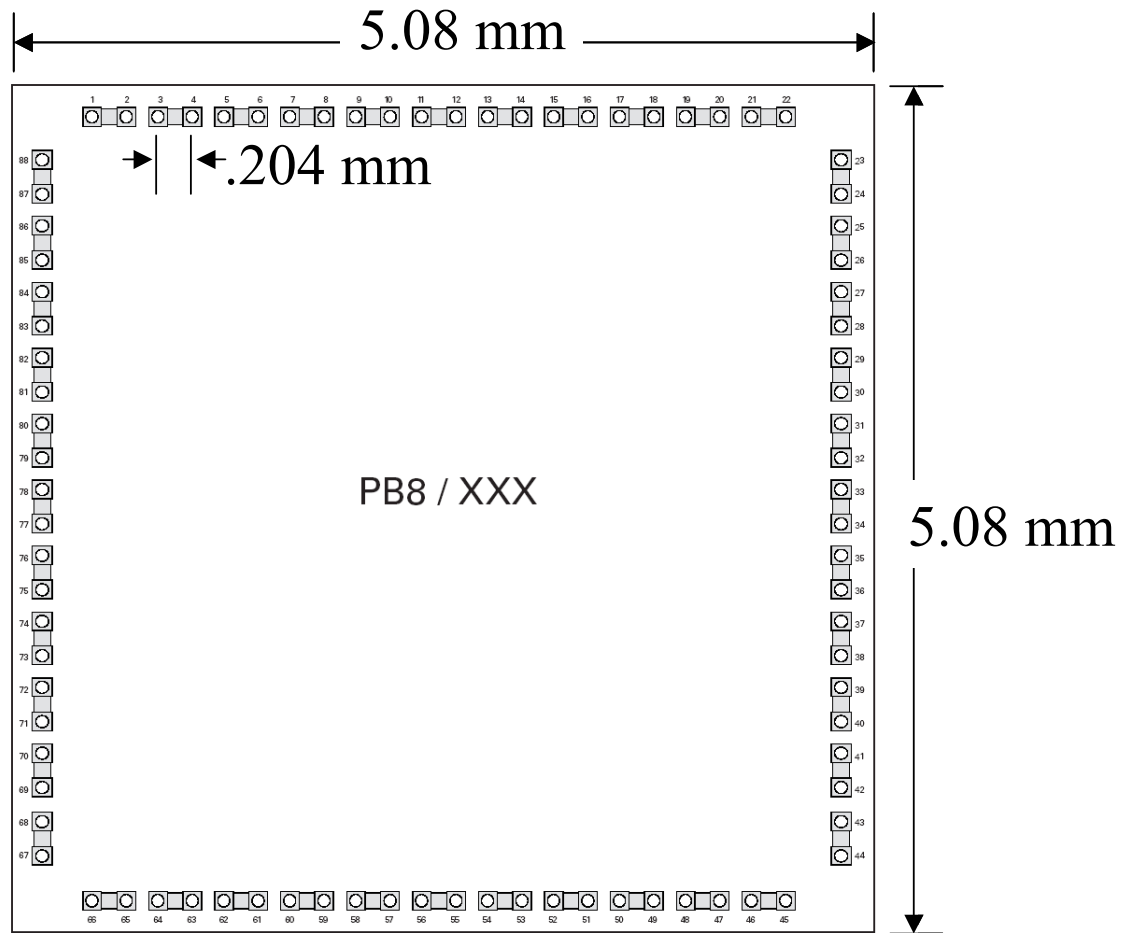


Figure 4-5 PB8 2x2 Test Die

Individual
bond pad

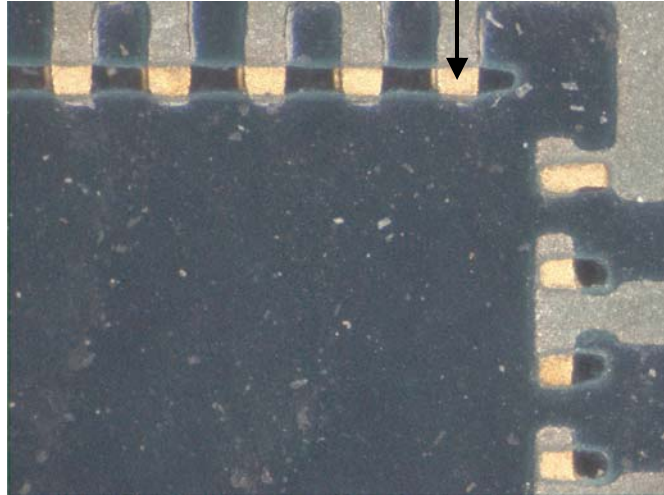


Figure 4-6 PB8 2x2 Individual Bond Pads

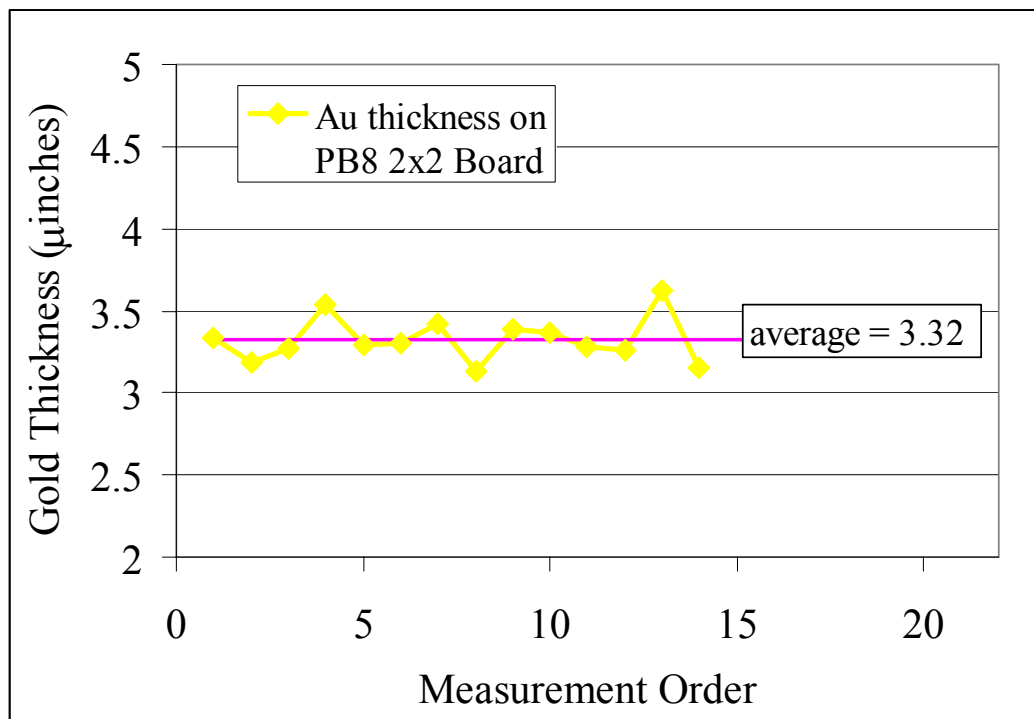


Figure 4-7 PB8 2x2 PCB Gold Metallization thickness (measured via XRF)

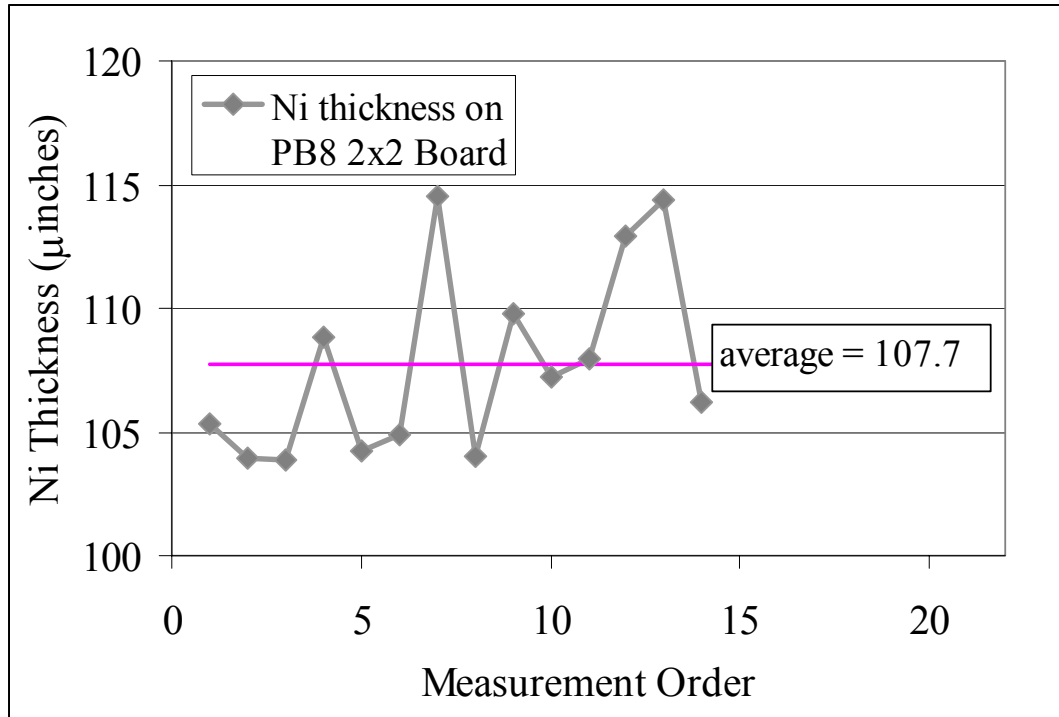


Figure 4-8 PB8 2x2 PCB Nickel Metallization thickness (measured via XRF)

4.1.1.2 PB6 2x2 Test Vehicle

The PB6-2x2 test vehicle is similar to the PB8-2x2 test vehicle, however it has a smaller pitch and smaller bumps with more I/O. The PB6-2x2 die was again mounted to a high- T_g substrate, with a glass transition temperature of 180 °C. The PB6-2x2 measured 5.08mm x 5.08mm (0.2 inches x 0.2 inches) in overall size, a total I/O count of 112 63Sn/37Pb flip chip bumps, and a bump to bump pitch of 150 microns. The bump diameter was 100 microns and the height of each individual bump was 85 microns, after collapse the standoff height for this flip chip was 25 microns. A general schematic of the PB8 2x2 test die is shown in Figure 4-11. There were two bond pad metallizations for this substrate: Cu/Ni/Au and Cu/OSP. The Cu/Ni/Au metallization was 0.043mm of copper, 4 microns of electroless Nickel (measurements in Figure 4-15), and an immersion

gold layer which was 0.218 microns thick on average (measurements in Figure 4-14). . The second metallization, Cu/OSP, consisted of 0.045 mm of copper and a layer of organic solderability preservative that ranged in thickness from 0.05 to 0.13 microns. The substrate bond pads were hybrid in nature with two sides that were solder mask defined, SMD, and two sides that were non-solder mask defined, NSMD. The overall shape of the bond pads was a rectangle (Figure 4-12).

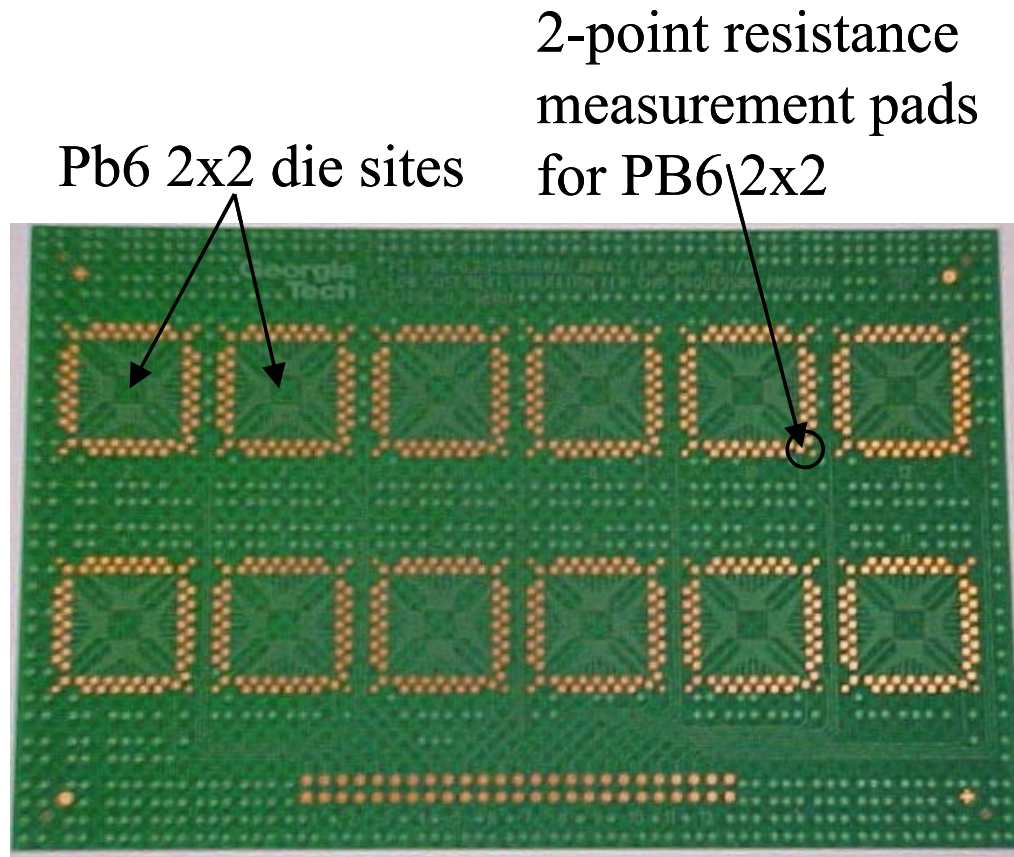


Figure 4-9 Substrate for PB6 2x2 Test Vehicle

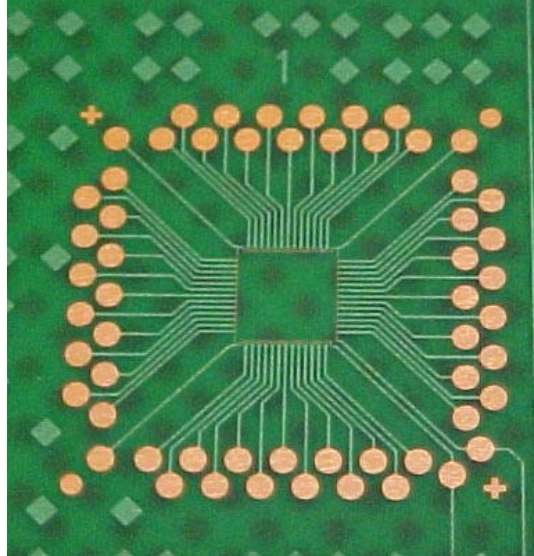


Figure 4-10 Close-Up View of a PB6 Die site on PCB

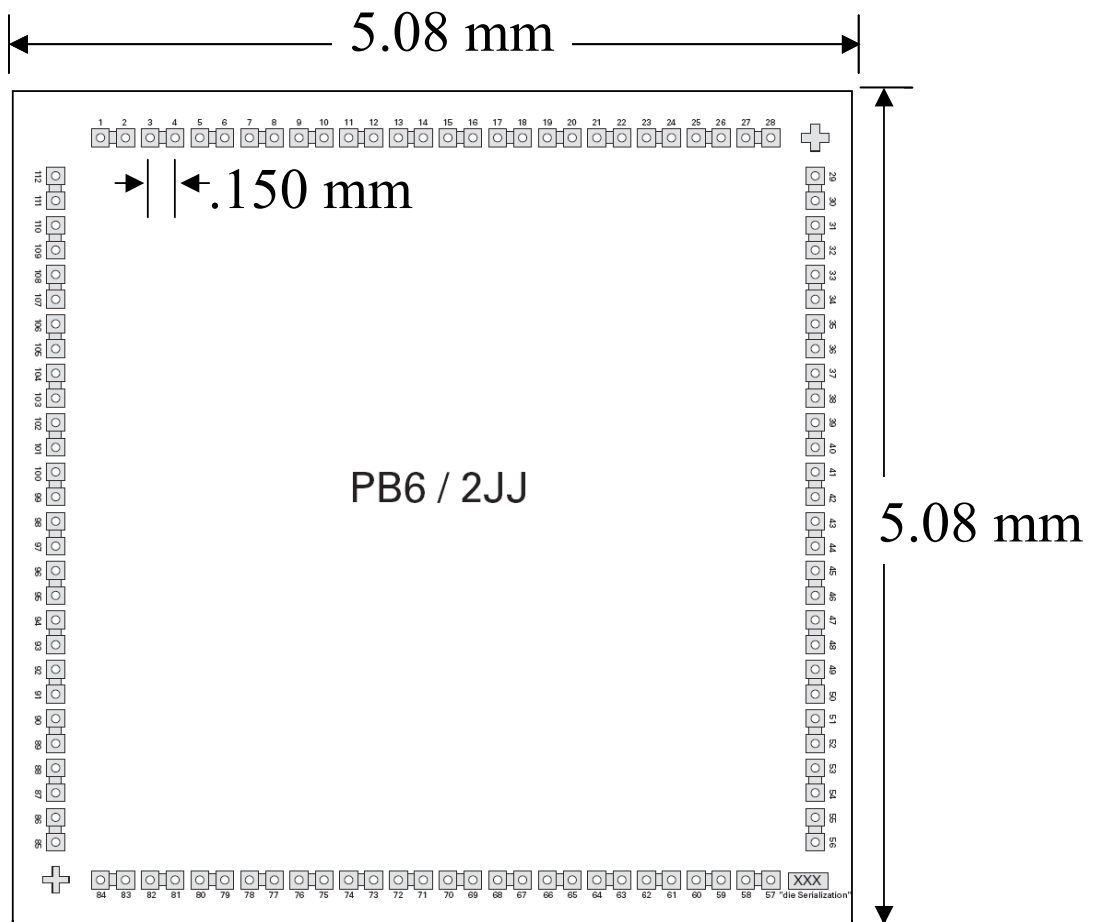


Figure 4-11 Schematic of PB6 Test Die

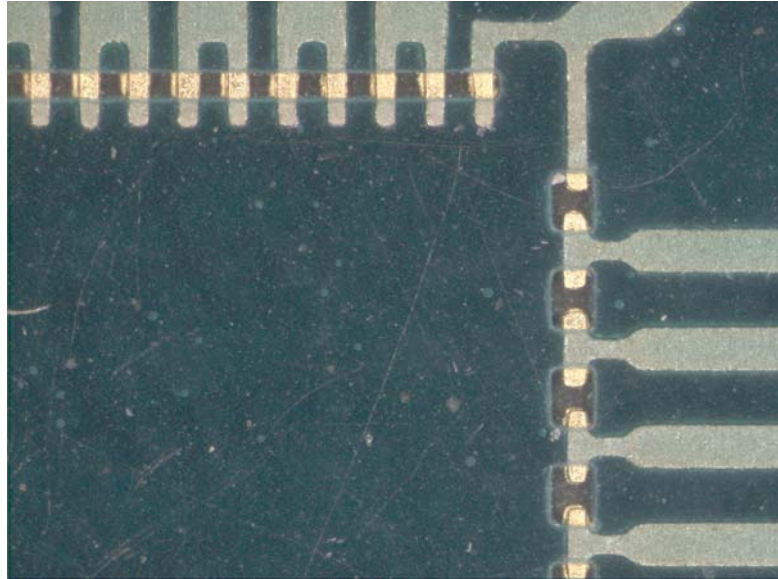


Figure 4-12 PB6 2x2 substrate pad openings

Individual
bond pad

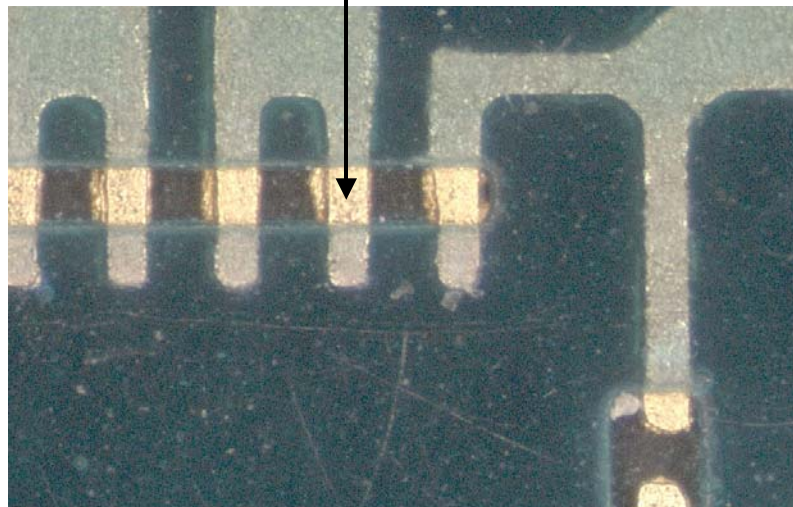


Figure 4-13 Individual bond site for a PB6 2x2 Test Vehicle

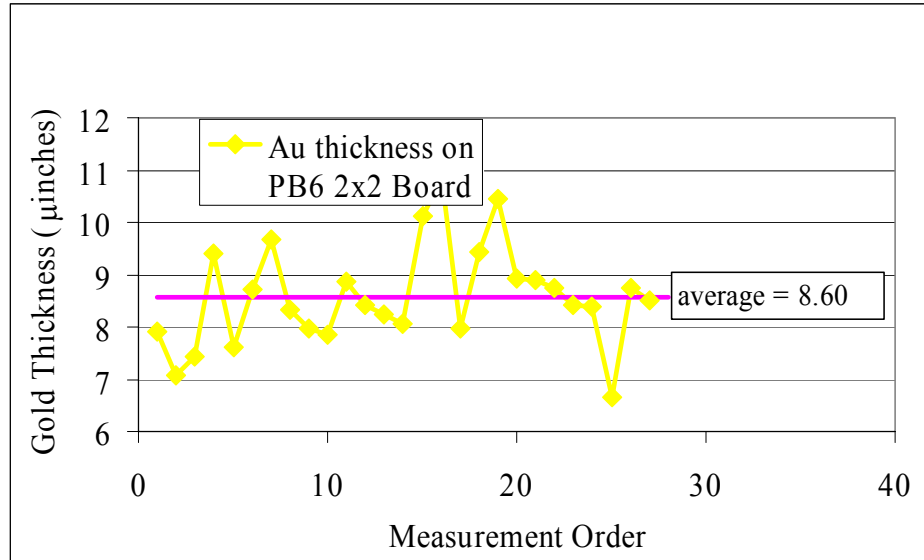


Figure 4-14 PB6 2x2 PCB Gold Metallization Thickness (measured via XRF)

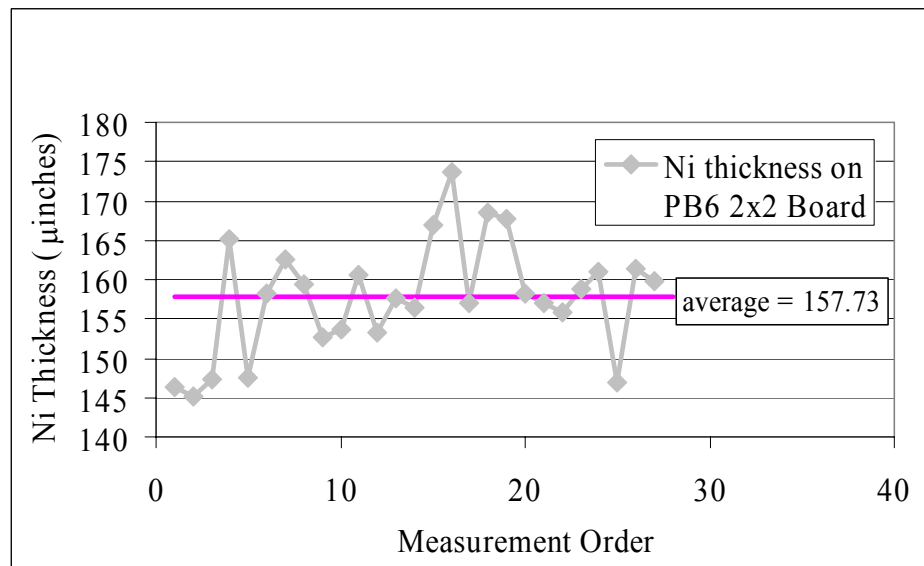


Figure 4-15 PB6 2x2 PCB Nickel Metallization Thickness (measured via XRF)

4.1.1.3 FA10 2x2 Siemens Test Vehicle

The FA10-2x2 test vehicle is a test vehicle that uses a full area array test die with 317 I/O which is about 3 times the I/O of the perimeter array test vehicles. The FA10-2x2 die was again mounted to a high-Tg substrate, with a glass transition temperature of

180 °C. The FA10-2x2 measured 5.08mm x 5.08mm (0.2 inches x 0.2 inches) in overall size, a total I/O count of 317 63Sn/37Pb flip chip bumps, and a bump to bump pitch of 254 microns. The bump diameter was 135 microns and the height of each individual bump was 110 microns, after collapse the standoff height for this flip chip was less than 110 microns. The general schematic of the FA10-2x2 test die is shown in Figure 4-20. There was one bond pad metallization for this substrate, Cu/Ni/Au. The Cu/Ni/Au metallization was 0.037mm of copper, 4.3 microns of electroless Nickel, and an immersion gold layer ranging in thickness from 0.05 to 0.30mm. There was no OSP metallization used on this substrate. The substrate bond pads were hybrid in nature with two sides that were solder mask defined, SMD, and two sides that were non-solder mask defined, NSMD. The overall shape of the bond pads was a rectangle.

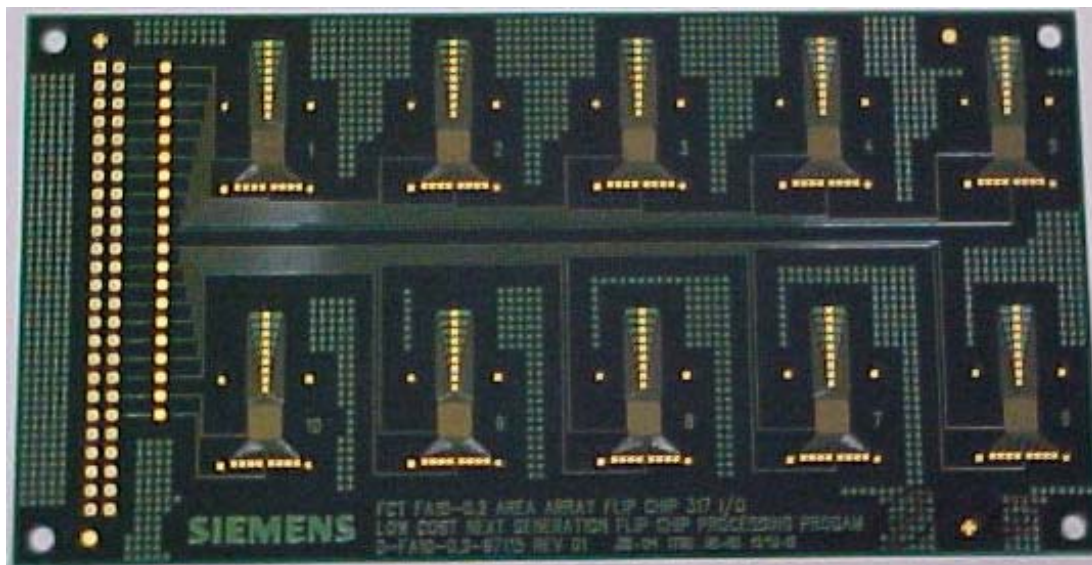


Figure 4-16 Substrate for FA10 2x2 Siemens Test Vehicle

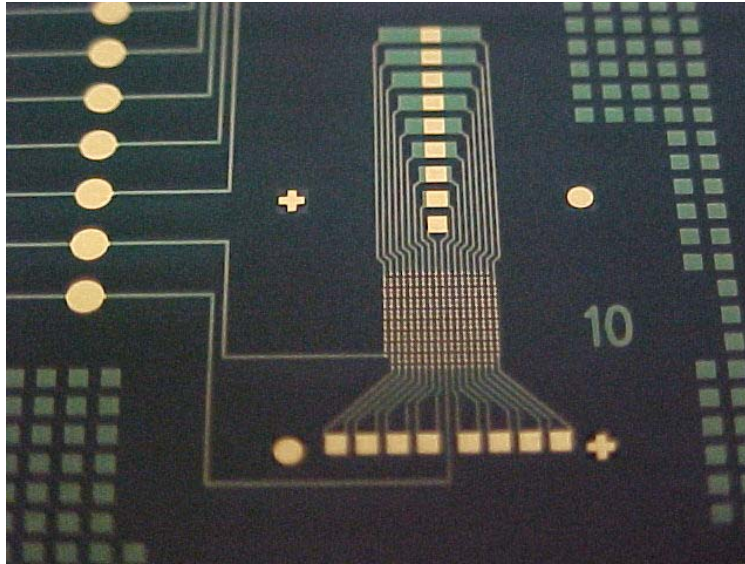


Figure 4-17 Close-Up View of a FA10 2x2 Die site on Siemens PCB

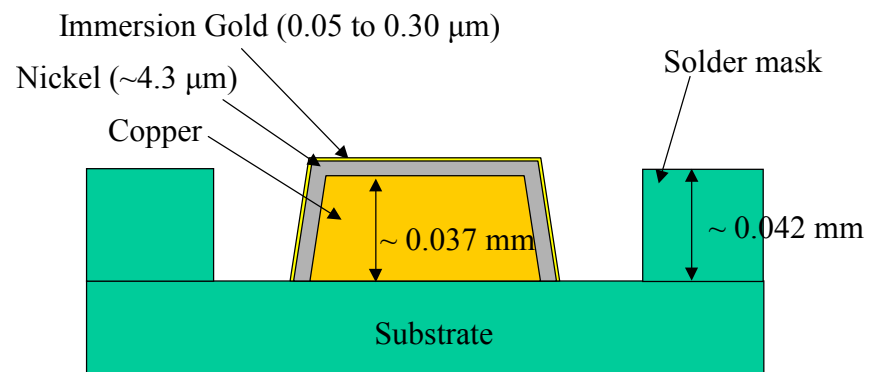


Figure 4-18 FA10 2x2 Siemens Boards Bond Pad Structure

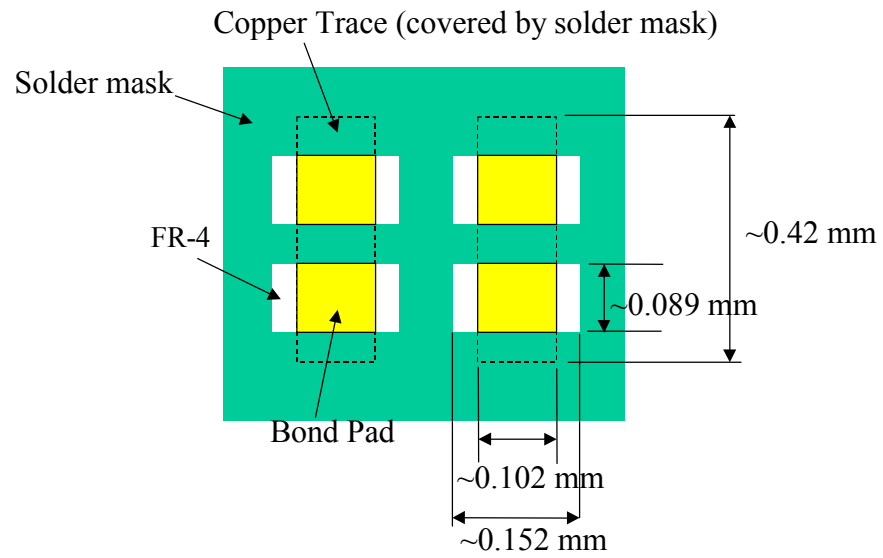


Figure 4-19 FA10 2x2 Bond Pads - Top View

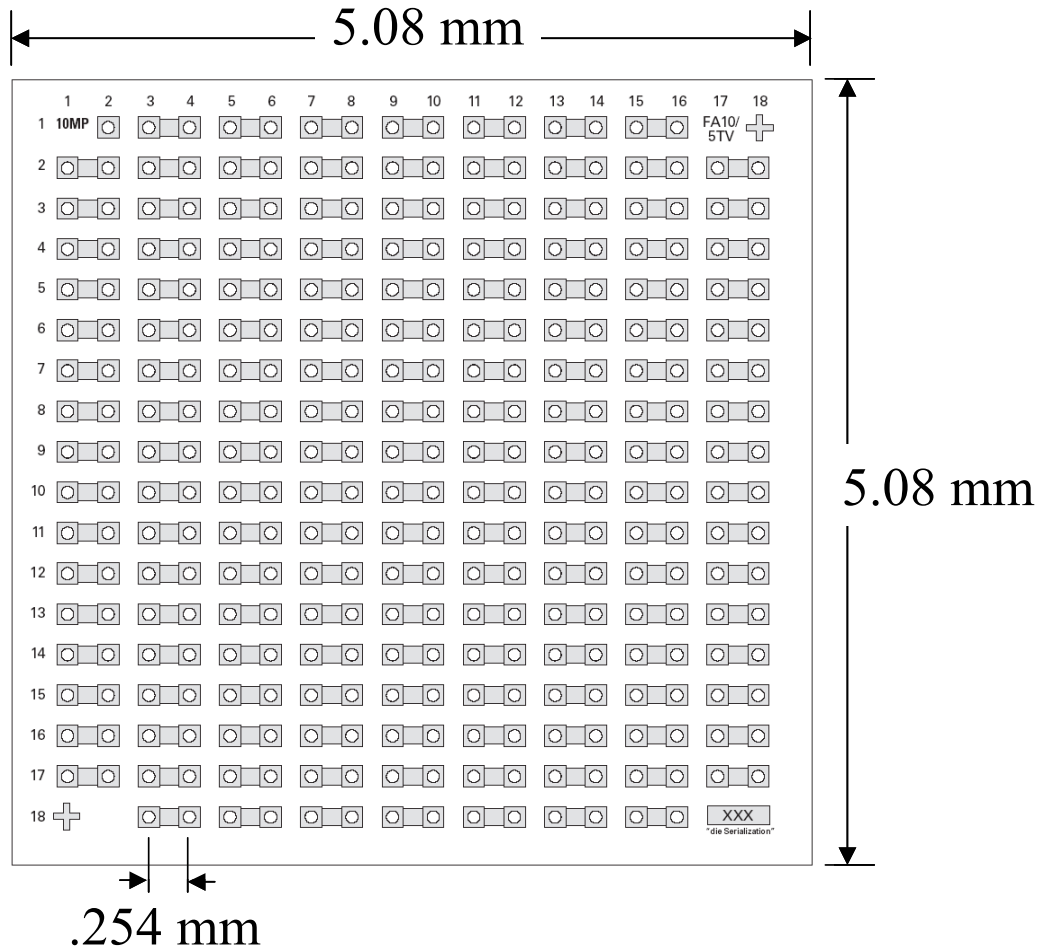


Figure 4-20 FA10 2x2 Test Die

4.1.1.4 FA10 2x2 and FA10 4x4 Test Vehicles

The FA10 2x2 test die was also placed on a second substrate with 10 flip chip bond sites and a v-groove between each of the flip chip sites to allow for easy removal of a single component. The FA10 2x2 was placed in the upper left-hand quadrant of the FA10 4x4 substrate bond pads. In addition, a FA10 4x4 was placed on this same substrate. The FA10 2x2 chip was 5.08mm x 5.08mm (0.2 inches x 0.2 inches) in overall size, and the FA10 4x4 was 10.16mm x 10.16mm (0.4 inches x 0.4 inches) in overall

size. The FA10 2x2 had 317 I/O, and the FA10 4x4 had 1268 I/O. The pitch of the I/O was 254 microns for each of the full area array test die. The bump height was 110 microns, and the bump diameter was 135 microns. The standoff height of the FA10 test vehicles was 66 microns (as measured from top of solder mask to bottom of die); and the final height of the solder joint after assembly was 87 microns (this was measured from the UBM to the top of the wettable pad). Again, the substrates had a glass transition temperature of 180 °C, and a board thickness of 0.7874mm.

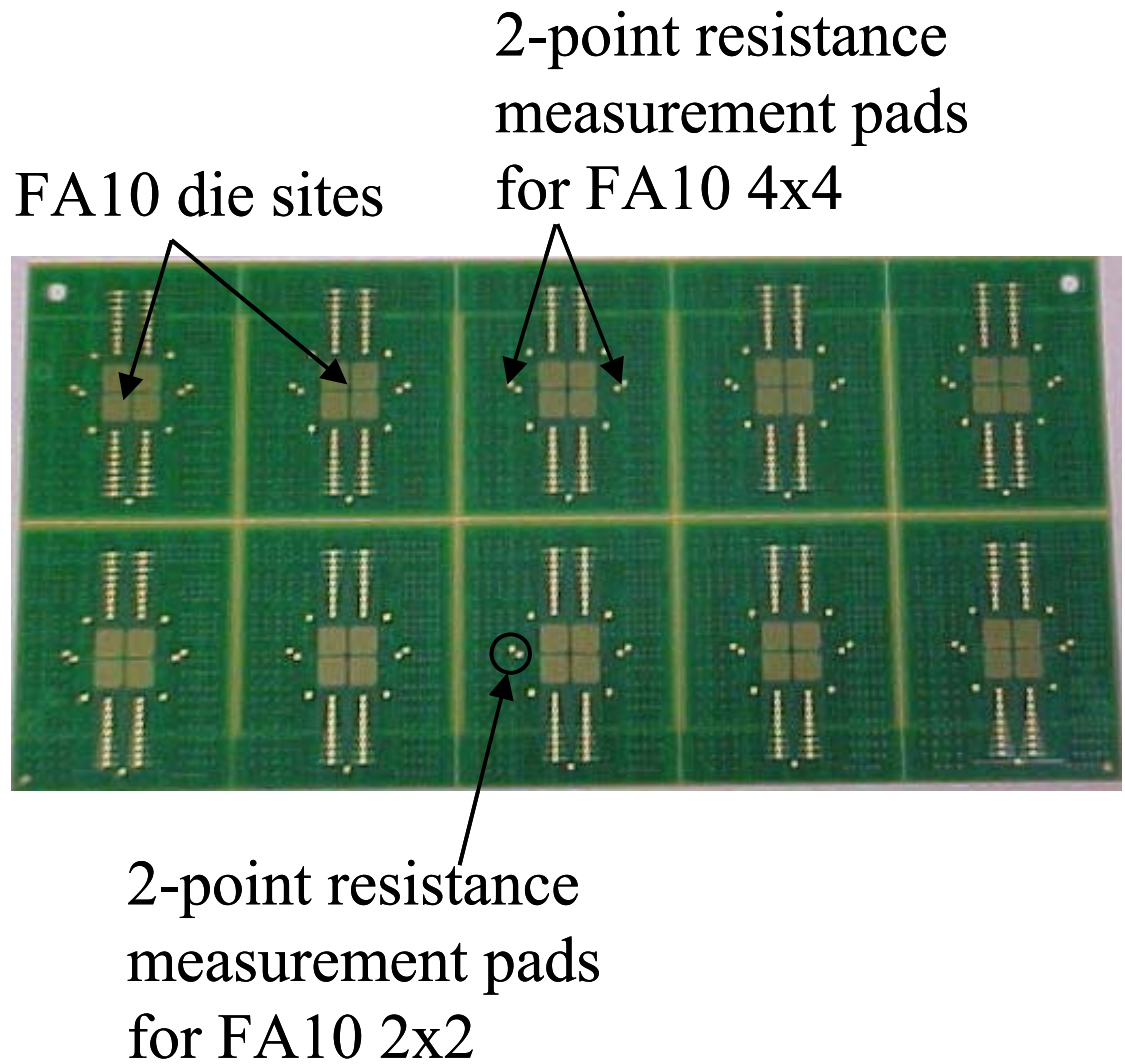


Figure 4-21 Substrate for FA10 2x2 and FA10 4x4 Test Vehicle

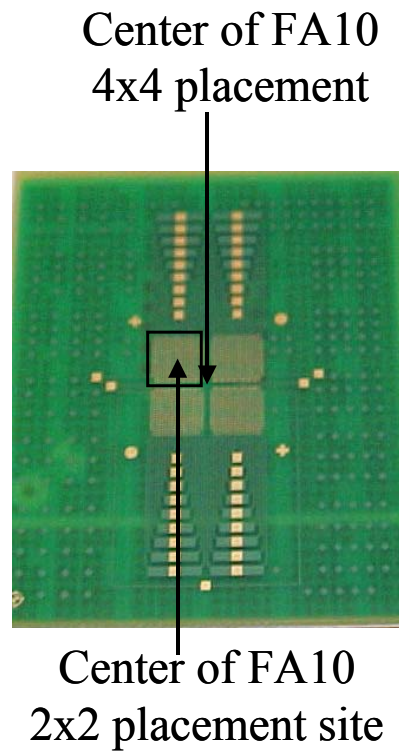


Figure 4-22 Close-Up View of a FA10 4x4 and FA10 2x2 Die site on PCB

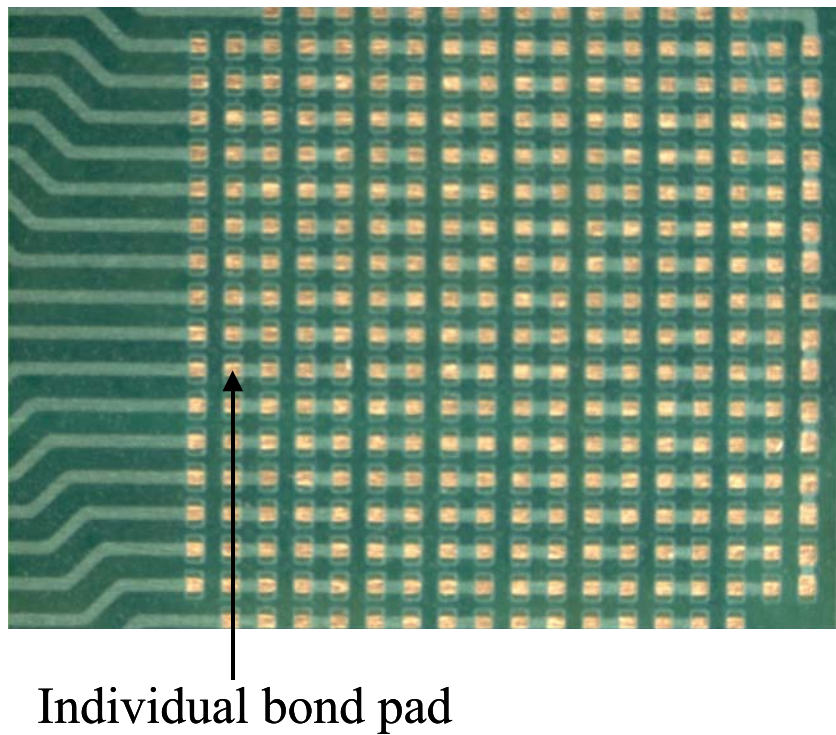
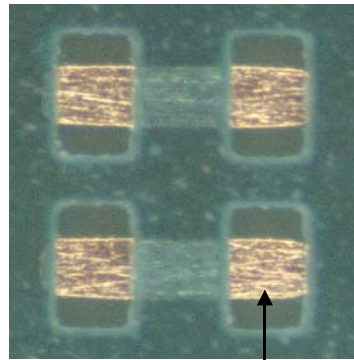


Figure 4-23 Image of an individual bond site for an Siemens FA10



Individual
bond pad

Figure 4-24 Image of an individual bond pad

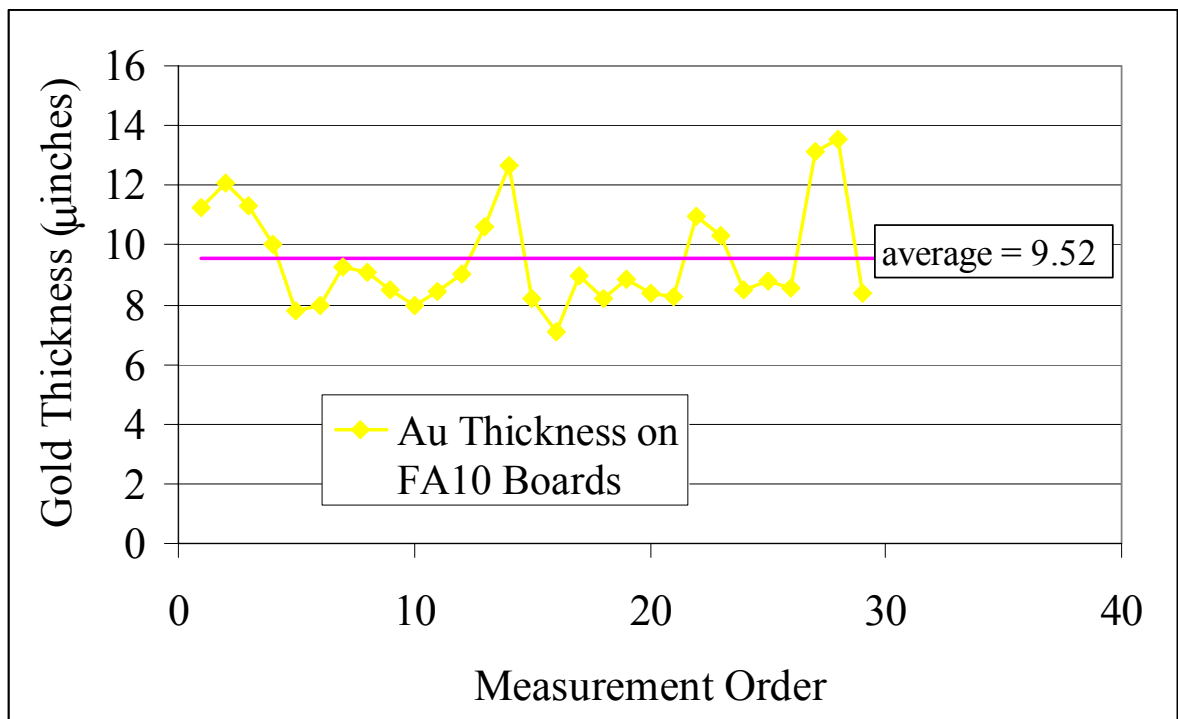


Figure 4-25 Siemens FA10 PCB Gold Metallization Thickness (measured via XRF)

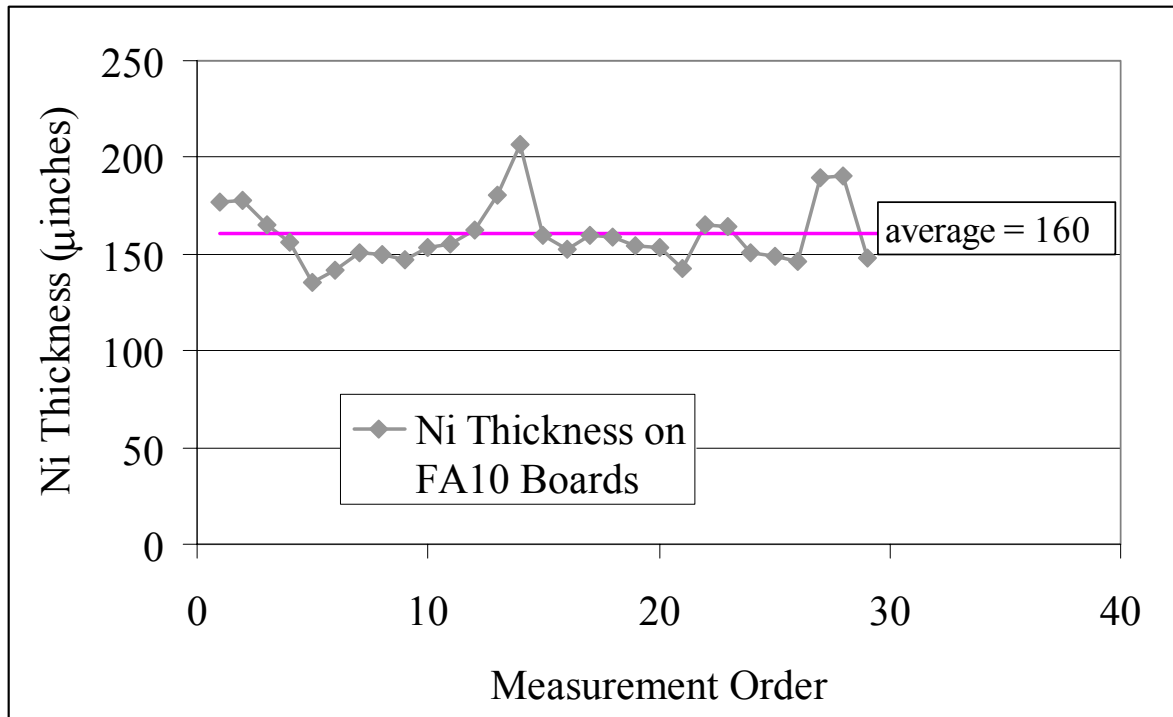


Figure 4-26 Siemens FA10 PCB Ni Metallization Thickness (measured via XRF)

4.1.1.5 Siemens AG FA10 2x2 Test Vehicles

The FA10 2x2 test die was also placed on a substrate with 6 flip chip bond sites and a v-groove between the flip chip sites to allow for easy removal of two flip chip packages at a time. The FA10 2x2 was placed on the die site shown in the figure below. The FA10 2x2 chip was 5.08mm x 5.08mm (0.2 inches x 0.2 inches) in overall size with 317 I/O. The pitch of the I/O was 254 microns for each of the full area array test die. The bump height was 110 microns and the bump diameter was 135 microns. The substrates had a glass transition temperature of 139 °C (as measured with DMA) and a board thickness of 1.46 mm.

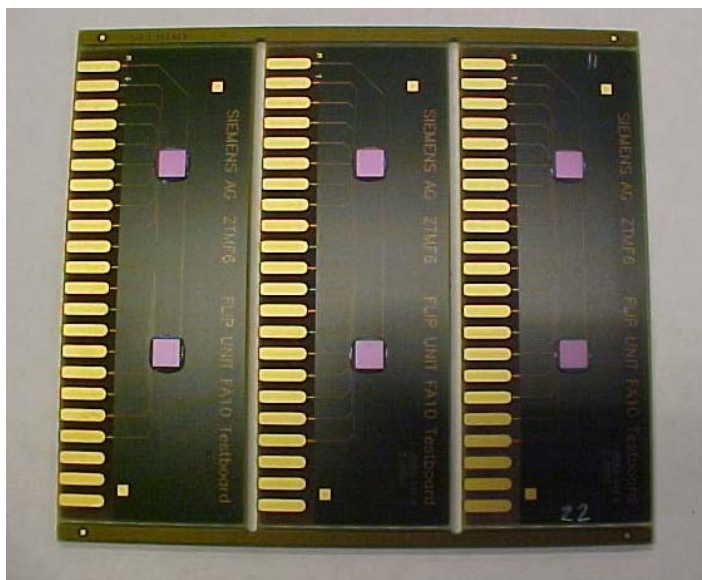


Figure 4-27 Siemens AG Substrate for FA10 2x2 Test Vehicle

Individual
bond pad

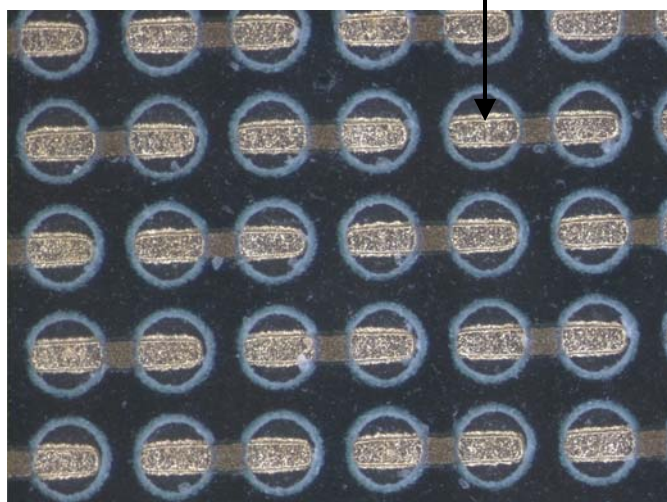


Figure 4-28 Siemens AG Test Boards Individual Bond Pads

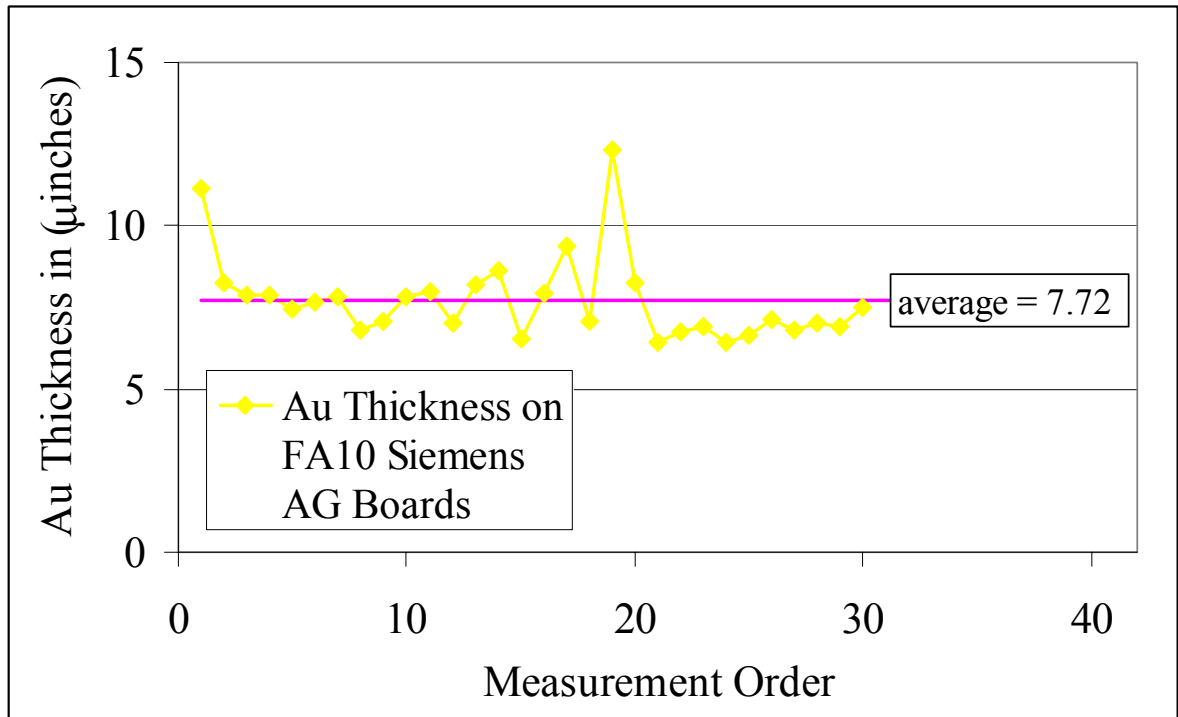


Figure 4-29 Siemens AG FA10 PCB Gold Metallization Thickness (measured via XRF)

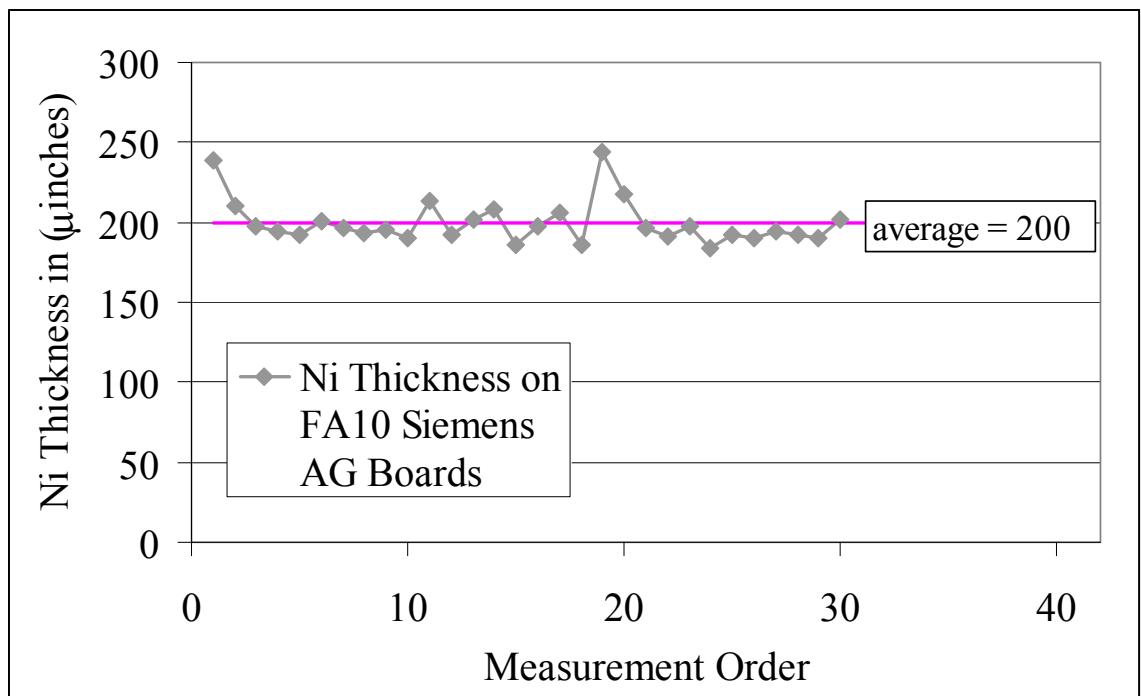


Figure 4-30 Siemens AG FA10 PCB Nickel Metallization Thickness (measured via XRF)

The next set of test vehicles was used by Thorpe [Thorpe, 1999]. They are included in this thesis for completeness simply because the reliability results for these test vehicles was included in the final regression analysis in the last section of Chapter 5.

4.1.1.6 RT - Test Vehicle 1

Test vehicle 1 used a perimeter array PB8-4 chip mounted on an FR-4 substrate with four die bond sites per board. The PB8-4 chip (Figure 4-31) was 10.16 x 10.16 mm and had 352 interconnects at a bump to bump pitch of 203 μ m. The substrate (Figure 4-32) had a T_g of 180 $^{\circ}$ C and a thickness of 0.7874 mm (0.031"). The bond pad metallization shown in Figure 4-33 was 0.045 mm of copper, 3.8 μ m of electroplated Nickel, and an immersion gold layer 0.05 to 0.30 μ m thick. The soldermask design, shown in Figure 4-34, consists of circular soldermask openings.

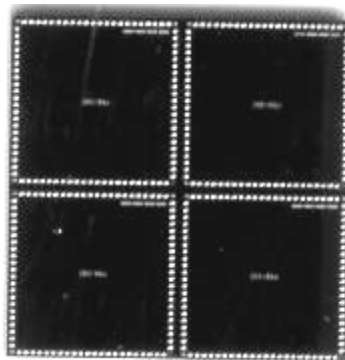


Figure 4-31 RT- Test Vehicle 1 - Chip Layout

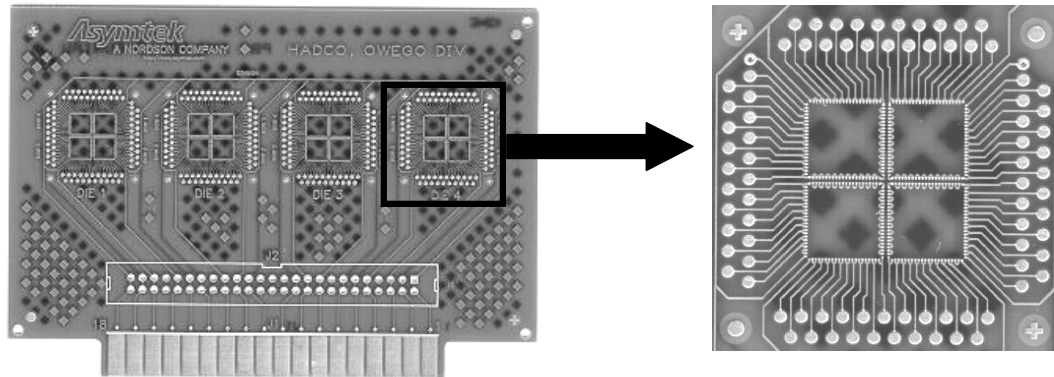


Figure 4-32 RT- Test Vehicle 1 - Substrate Layout

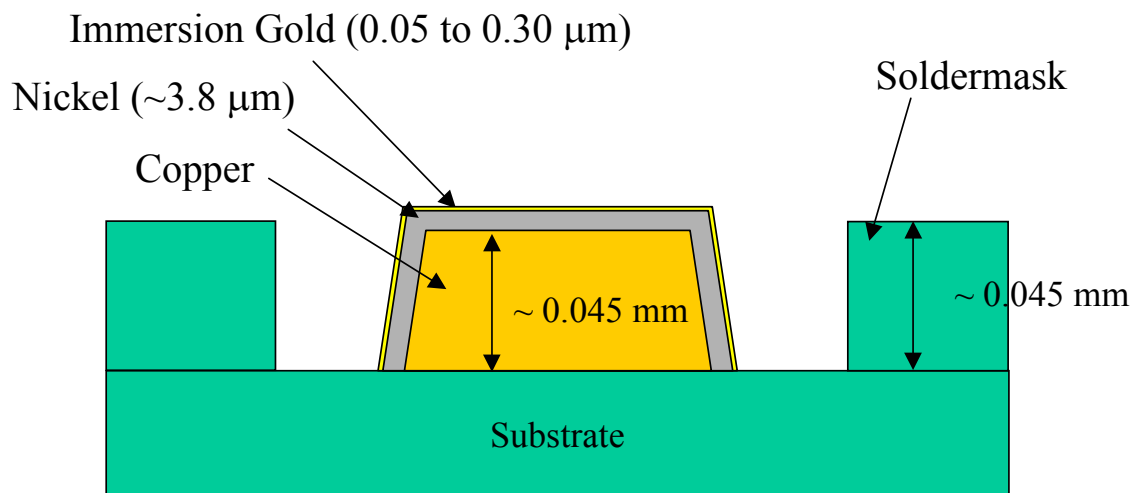


Figure 4-33 RT- Test Vehicle 1 – Bond Pad Structure

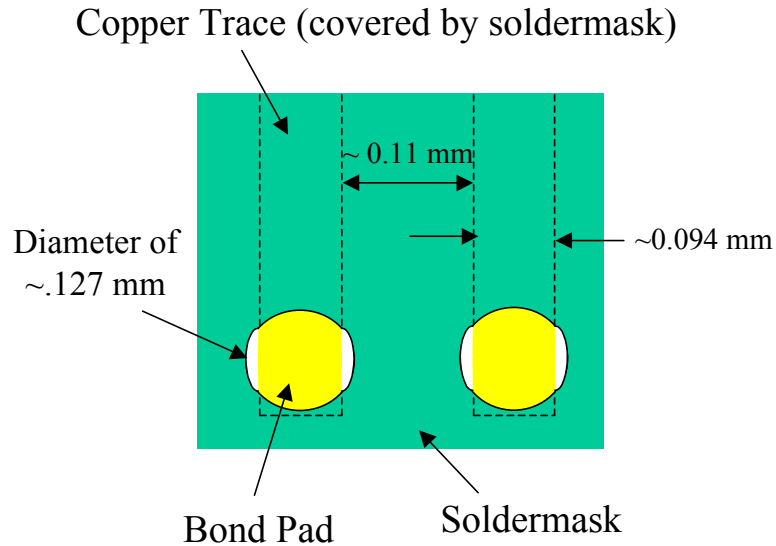


Figure 4-34 RT- Test Vehicle 1 – Soldermask Design

4.1.1.7 RT - Test Vehicle 2

Test vehicle 2 utilized a perimeter array PB8-4 chip mounted on an FR-4 substrate with four die bond sites per board. The PB8-4 chip (Figure 4-35) was 10.16 x 10.16 mm and had 352 interconnects at a bump to bump pitch of 203 μ m. The substrate (Figure 4-36) had a T_g of 180 $^{\circ}$ C and a thickness of 0.7874 mm (0.031"). The bond pad metallization shown in Figure 4-37 was 0.045 mm of copper, 3.8 μ m of electroplated Nickel, and an immersion gold layer 0.05 to 0.30 μ m thick. The soldermask design (Figure 4-38) consisted of a continuous "trench" opening and produced square bond pads.

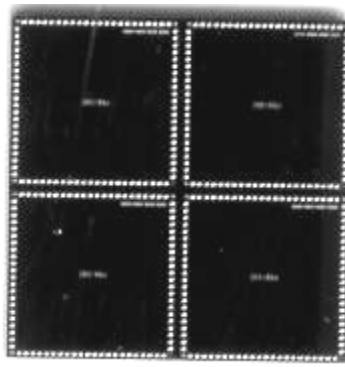


Figure 4-35 RT- Test Vehicle 2 – Chip Layout

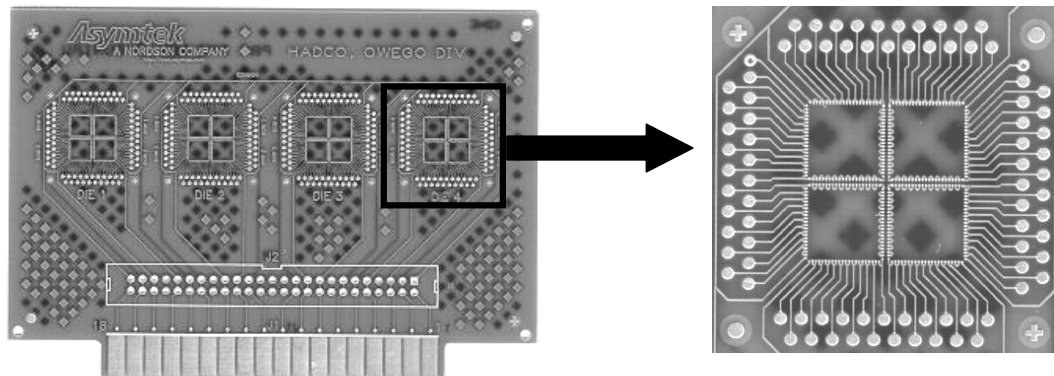


Figure 4-36 RT- Test Vehicle 2 - Substrate Layout

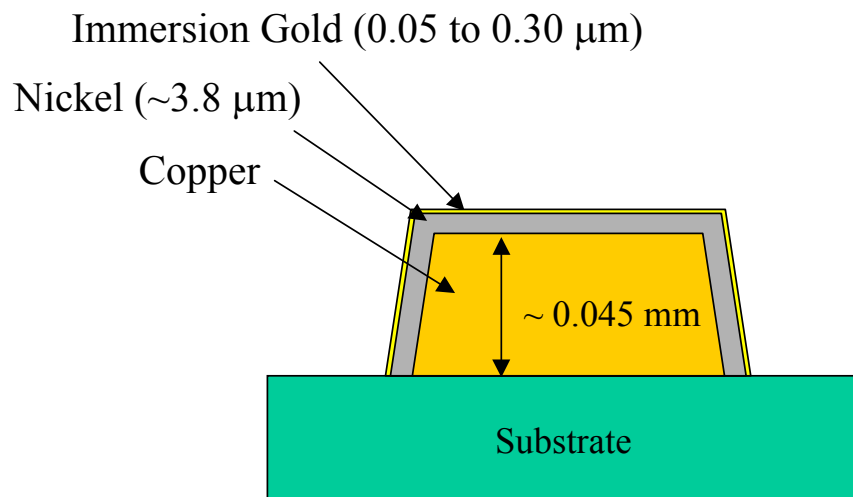


Figure 4-37 RT- Test Vehicle 2 – Bond Pad Structure

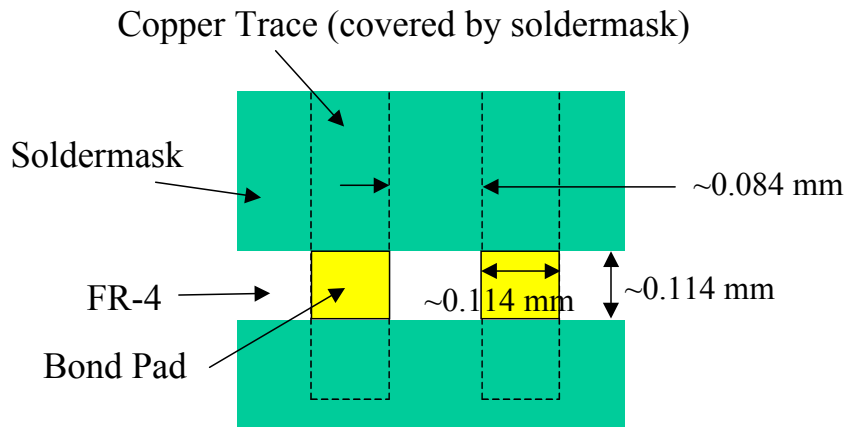


Figure 4-38 RT- Test Vehicle 2 – Soldermask Design

4.1.1.8 RT - Test Vehicle 3

Test vehicle 3 used a perimeter array PB8-4 chip mounted on an FR-4 substrate with four die bond sites per board. The PB8-4 chip (Figure 4-39) was 10.16 x 10.16 mm and had 352 interconnects at a bump to bump pitch of 203 μ m. The substrate (Figure 4-40) had a T_g of 180 $^{\circ}$ C and a thickness of 0.7874 mm (0.031"). The bond pad metallization shown in Figure 4-41 consisted of 0.045 mm of copper and a layer of organic surface protectant (OSP) 0.05 to 0.13 μ m in thickness. The soldermask design (Figure 4-42) consisted of circular soldermask openings.

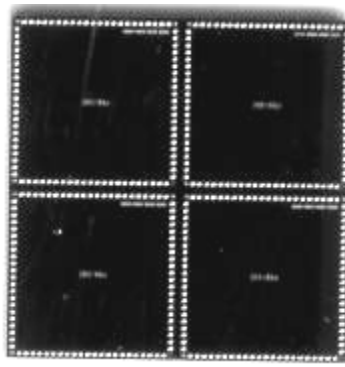


Figure 4-39 RT- Test Vehicle 3 – Chip Layout

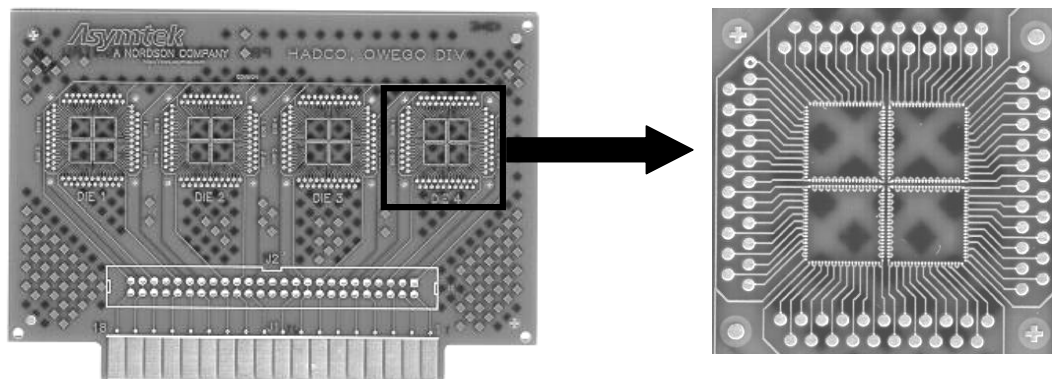


Figure 4-40 RT- Test Vehicle 3 - Substrate Layout

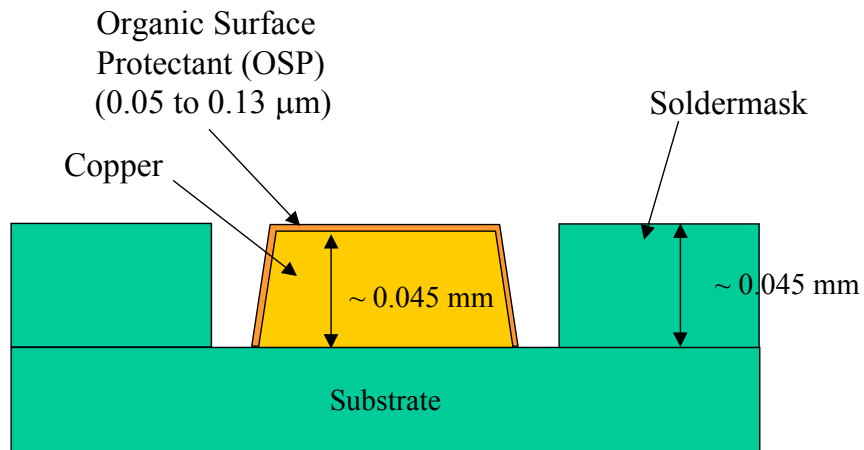


Figure 4-41 RT- Test Vehicle 3 – Bond Pad Structure

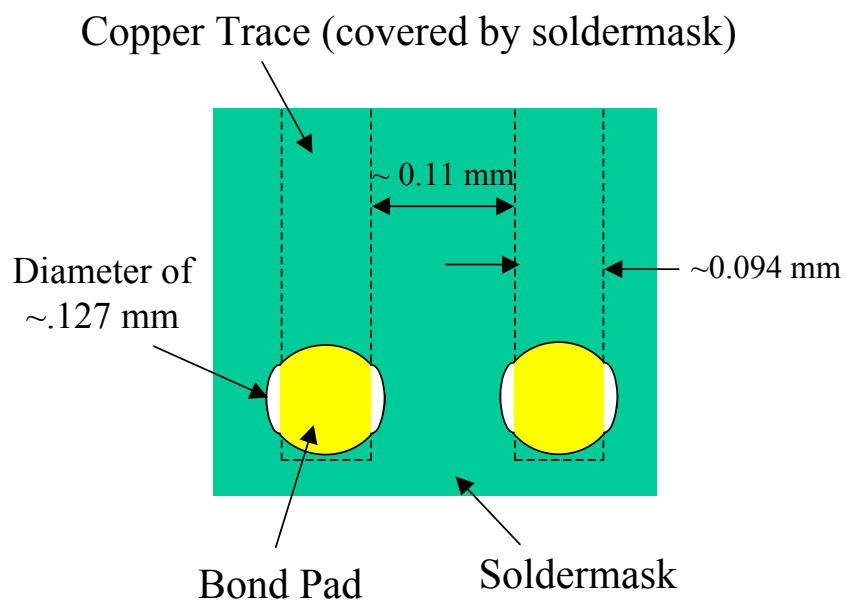


Figure 4-42 RT- Test Vehicle 3 – Soldermask Design

4.1.1.9 RT - Test Vehicle 4

Test vehicle 4 utilized a perimeter array PB8-2 chip mounted on an FR-4 substrate with 10 die bond sites. The PB8-2 chip (Figure 4-43) was 5.08 x 5.08 mm and had 88 interconnects at a bump to bump pitch of 203 μ m. The substrate (Figure 4-44) had a T_g of 180 $^{\circ}$ C and a thickness of 0.7874 mm (0.031"). The bond pad metallization shown in Figure 4-45 consisted of 0.043 mm of copper, 3.8 μ m of electroplated Nickel, and an immersion gold layer 0.05 to 0.30 μ m thick. The soldermask design (Figure 4-46) consisted of rectangular soldermask openings, which produced rectangular bond pads.

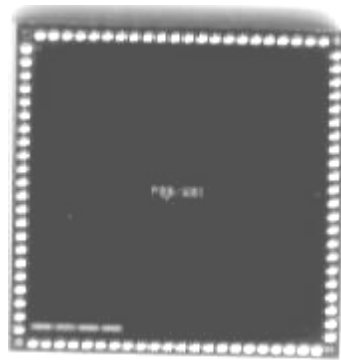


Figure 4-43 RT- Test Vehicle 4 – Chip Layout

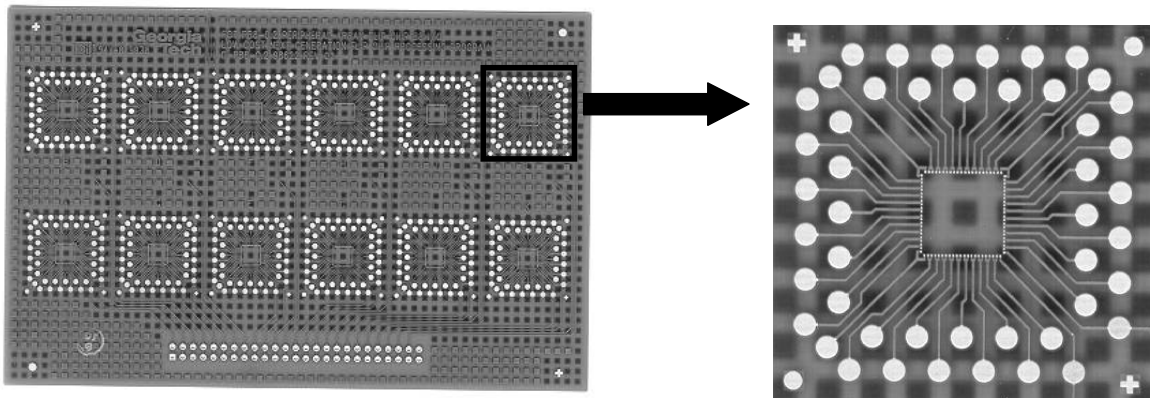


Figure 4-44 RT- Test Vehicle 4 - Substrate Layout

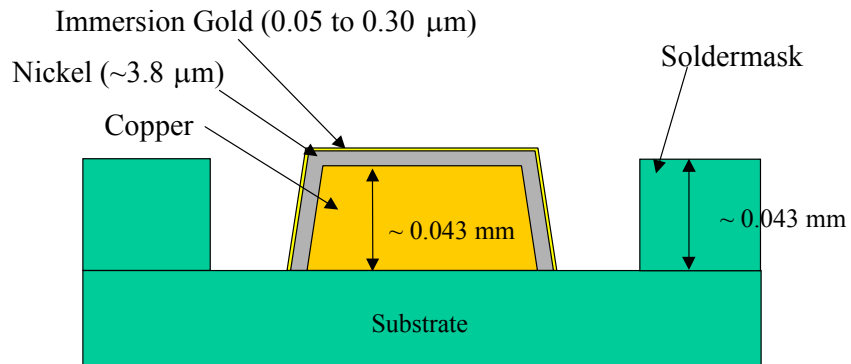


Figure 4-45 RT- Test Vehicle 4 – Bond Pad Structure

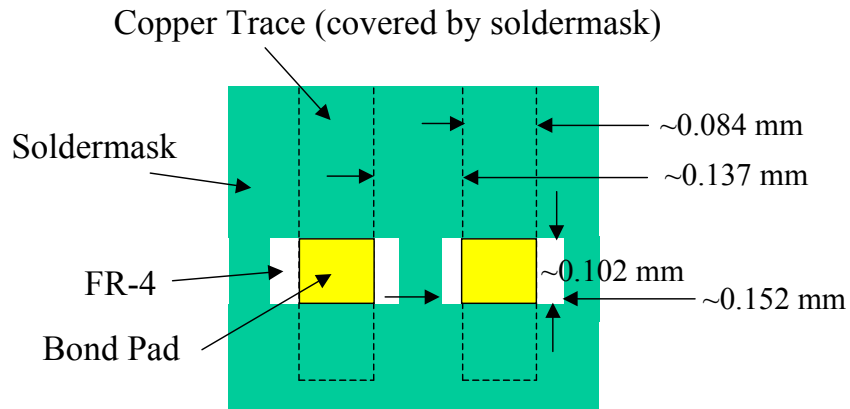


Figure 4-46 RT- Test Vehicle 4 – Soldermask Design

4.1.1.10 RT - Test Vehicle 5

Test vehicle 5 utilized a full area array FA10-4 chip mounted on a 0.7874 mm (0.031") thick FR-4 substrate with three chip bond sites. The FA10-4 chip (Figure 4-47) was 10.16 x 10.16 mm and had 1268 interconnects at a bump to bump pitch of 254 μm . The substrate (Figure 4-48) had a T_g of 180 $^{\circ}\text{C}$ and a thickness of 0.7874 mm (0.031"). The bond pad metallization shown in Figure 4-49 consisted of 0.034 mm of

copper, 4.3 μm of electroplated Nickel, and an immersion gold layer 0.05 to 0.30 μm thick. The soldermask design (Figure 4-50) consisted of rectangular soldermask openings, which produced rectangular bond pads.

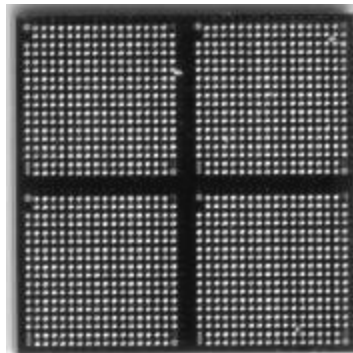


Figure 4-47 RT- Test Vehicle 5 – Chip Layout

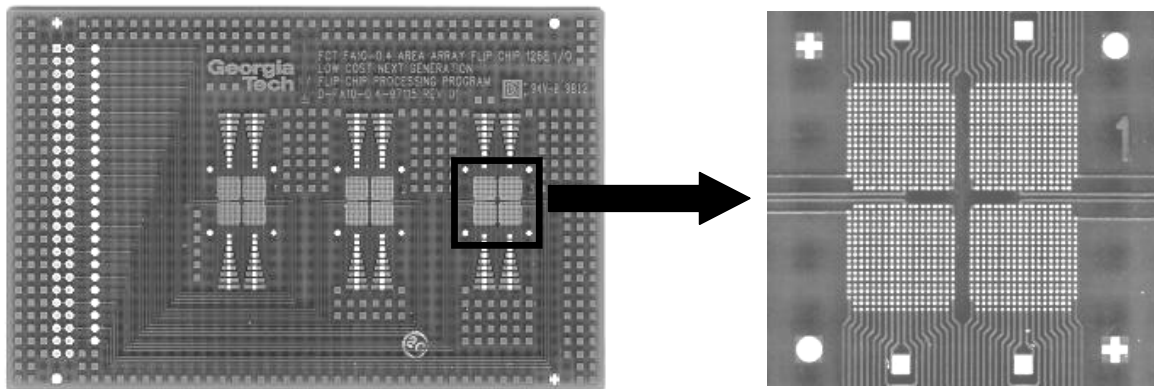


Figure 4-48 RT- Test Vehicle 5 - Substrate Layout

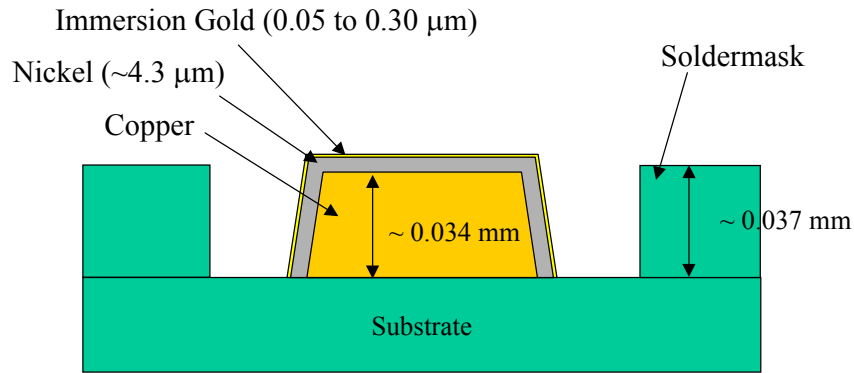


Figure 4-49 RT- Test Vehicle 5 – Bond Pad Structure

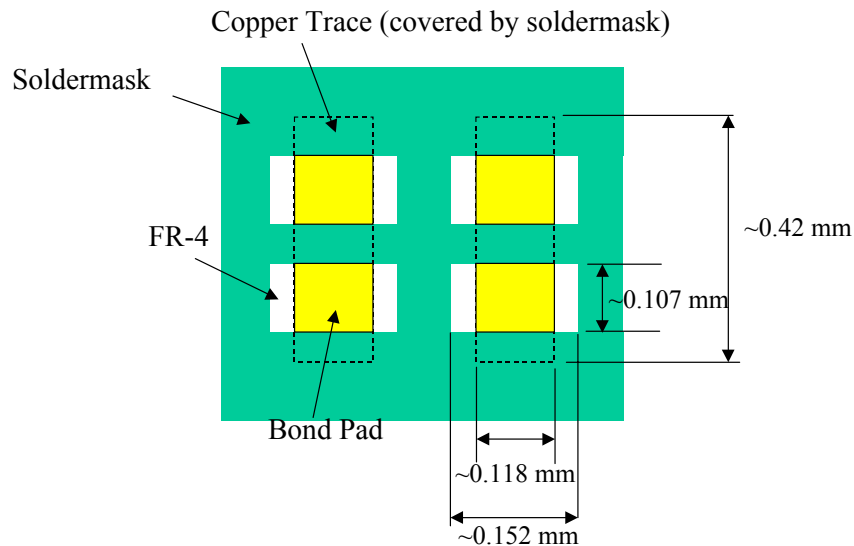


Figure 4-50 RT- Test Vehicle 5 – Soldermask Design

4.1.1.11 RT - Test Vehicle 6

Test vehicle 6 utilized a full area array FA10-2 chip mounted on a 0.031" thick FR-4 substrate with 10 chip bond sites. The FA10-2 chip (Figure 4-51) was 5.08 x 5.08 mm and had 317 interconnects at a bump to bump pitch of 254 μ m. The substrate (Figure 4-52) had a T_g of 180 $^{\circ}$ C and a thickness of 0.7874 mm (0.031"). The bond pad

metallization shown in Figure 4-53 consisted of 0.037 mm of copper, 4.3 μm of electroplated Nickel, and an immersion gold layer 0.05 to 0.30 μm thick. The soldermask design (Figure 4-54) consisted of rectangular soldermask openings, which produced rectangular bond pads.

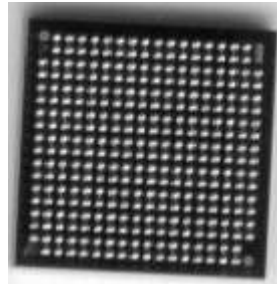


Figure 4-51 RT-Test Vehicle 6 – Chip Layout

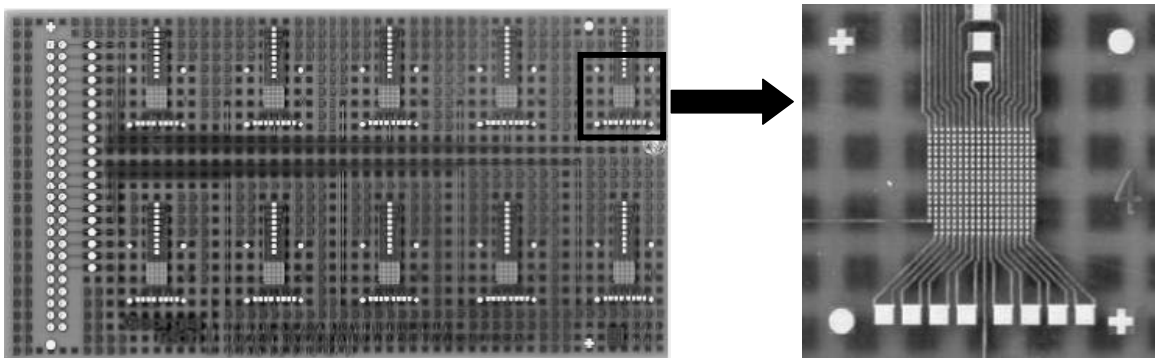


Figure 4-52 RT-Test Vehicle 6 - Substrate Layout

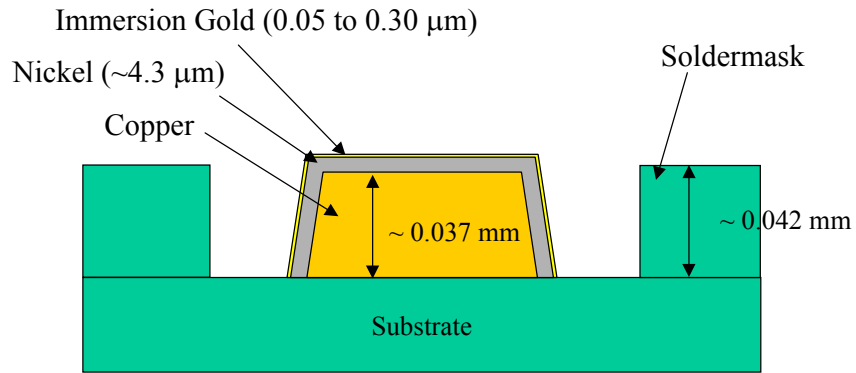


Figure 4-53 RT- Test Vehicle 6 – Bond Pad Structure

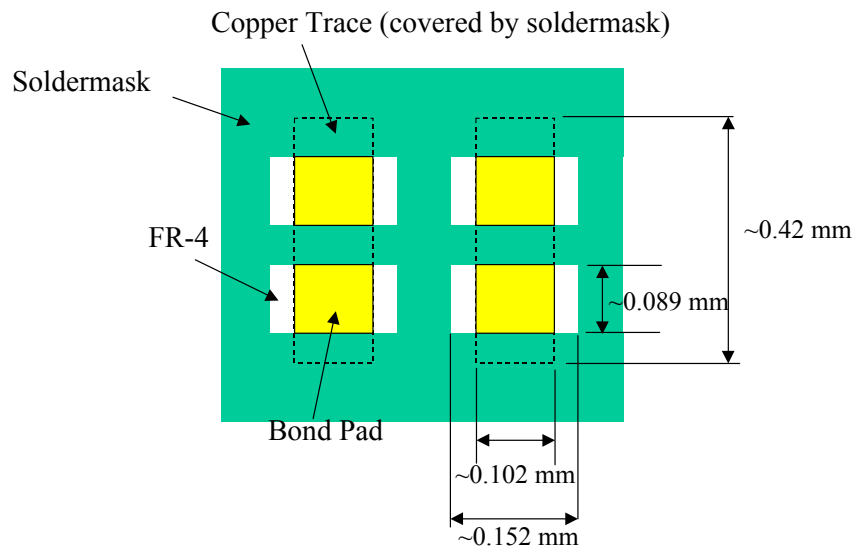


Figure 4-54 RT- Test Vehicle 6 – Soldermask Design

4.1.2 Assembly Information

The process characterization efforts completed by Lazarakis resulted in an optimized assembly process for the various experimental test vehicles used throughout the experimental portion of this research [Lazarakis, 2003]. The assembly process used

to generate the test vehicles described in Sections 4.1.1.1-4.1.1.4 for the reliability modeling effort will be outlined in this section, other information about process characterization efforts is presented by Lazarakis [Lazarakis, 2003]. Assembly information for the test vehicle described in Section 4.1.1.5 is presented by Colella [Colella, 2004]. Assembly information for test vehicles described in Sections 4.1.1.6-4.1.1.11 is described by Thorpe [Thorpe, 1999].

The general assembly flow (for test vehicles presented in Sections 4.1.1.1-4.1.1.4) is as follows: the boards were baked at 125 °C for 2 hours, no-flow underfill was dispensed in a dot pattern in the center of each of the bond pads with a CAMALOT 3700, flip chips were placed with a Siemens F5 DCA placement machine, and the assemblies were sent through a thermal profile in a BTU Paragon Reflow oven. Since no-flow underfill was used throughout this experimental work the reflow process served to cure the underfill (a thermosetting polymer) and form the flip chip solder joints. Specifics about the assembly process are presented in the remained Sections of 4.2.1 as well as Section 4.3.1.

4.1.2.1 Underfill Dispense Process

The no-flow underfill was dispensed with a SPEEDLINE CAM/ALOT Model # 3700. A 22 gage needle was used as the dispensing tool for all underfill deposits. The underfill was stored at -40°C prior to assembly; and was moved to room temperature about 30 minutes prior to assembly. This allowed the underfill time to thaw before processing. The underfill was dispensed in a ‘dot’ pattern, meaning that a small dot of

underfill was dispensed in the center of the die location. Roughly 8.5mg of underfill was dispensed for the 5mm die and 21mg of underfill for the 10mm die, amounts of underfill for the die used are shown in Table 4-5. The program used to dispense the underfill is shown in Table 4-1.

Table 4-1 Underfill Dispense Program for a ‘Dot’ Pattern

Step	Pattern	V	S	UP	DOWN
1	REFPT				
2	REFPT				
3	ZSENSE	1	4	30	1
4	MOVE	1	4	2	1
5	ZLINE	1	1	2	1
6	CLEAN	1	1	3	2
7	END				

The amount of underfill dispensed depended on the size of the die, the number of solder bumps on the flip chip, and the amount of underfill desired in the underfill fillet. The 5.08mm x 5.08mm die required between 8.0mg and 9.0mg of underfill, where as the 10.16mm x 10.16mm die required 21.0mg of underfill. Again, the details are shown in Table 4-5.

4.1.2.2 Placement Process

After the underfill had been dispensed, the flip chips were placed with a Siemens F5 DCA placement machine. There is no additional flux application because no-flow underfill has fluxing agents in the formulation that perform the required reduction reaction with oxides on the wettable surfaces. In general, the Siemens placement

machine process flow is as follows: the test vehicles enter the Siemens machine on a conveyer mechanism, the substrate moves along the conveyor rails until it reaches the placement station, the machine clamps the board in place, the fiducial camera reads all necessary fiducials, the IC head picks the required test die out of the component waffle pack tray, visions the flip chip bumps, and places the chip with a given force on the die site. Once all die have been placed, the substrate exits the machine via the conveyer belts. All die on the substrate were then inspected using a Fein Focus X-ray machine.

4.1.2.3 Reflow Process

Once the flip chip was placed and the placement accuracy of the chip was verified via X-ray analysis, the substrate was sent through a reflow oven such that the flip chip solder joints formed and the no-flow underfill cross linked. The reflow process is critical to a good final assembly for no-flow fluxing underfills. The reflow process is where the underfill, which is a thermosetting polymer, cures and the flip chip solder interconnects form. It is critical that the underfill layer does not pre-gel prior to the formation of the solder interconnects; this could cause a significant chip yield loss. On the other hand, the underfill must be cured to a given level – this is quantified as a percent of cross linking which can be determined with DSC (Differential Scanning Calorimetry).

The test vehicles were reflowed in a BTU Paragon 98N reflow oven with 7 independent thermal zones, these zones allowed for convection to the top and the bottom of the substrate. The reflow profiling was performed with a Slim KIC2000 thermal profiling system. The KIC thermal profiling system reported temperatures that were

measured on the actual substrate as it progressed through the reflow oven; thermocouples were mounted between the die and the substrate such that the actual profile the solder experiences would be obtained. Omega Engineering, K-type, thermocouples were used throughout the reflow characterization effort; these thermocouples are accurate to +2.2 °C to -2.2°C. The final reflow process selected was chosen based on the yield of the die as well as the percentage area of voiding on the resulting assemblies. The final reflow process is shown in Figure 4-55.

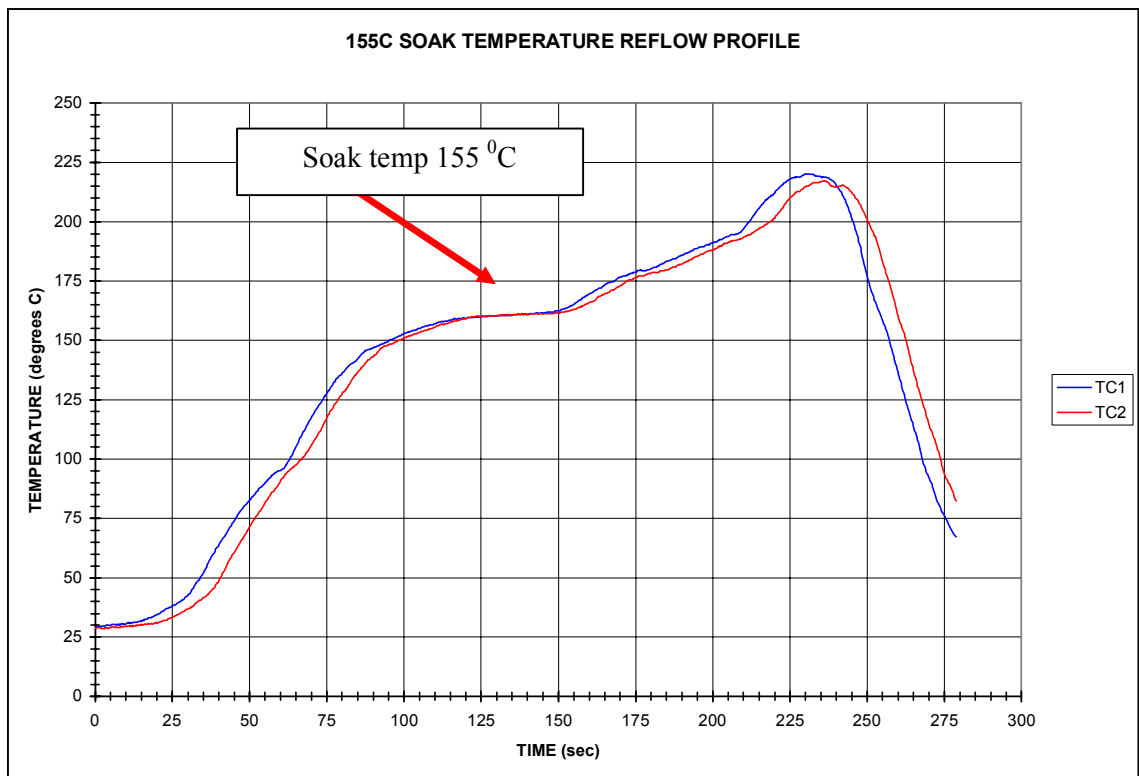


Figure 4-55 Reflow Profile Used for First 3000 Test Vehicles

The settings in the individual reflow zones are shown in Table 4-2.

Table 4-2 Reflow Zone Settings for the 7 Zone BTU Reflow Oven

Profile Name	Zone #1	Zone #2	Zone #3	Zone #4	Zone #5	Zone #6	Zone #7	Belt Speed
Soaktemp 155 °C	107.6 °C	168.1 °C	163.2 °C	161.1 °C	201.6 °C	201.0 °C	245.5 °C	28.4 (in/min)

4.1.2.4 C-Mode Scanning Acoustic Microscopy (CSAM)

All test vehicles were scanned using C-mode scanning acoustic microscopy. Scanning acoustic microscopy is capable of viewing cracks or delamination on the die/underfill surface as well as die cracking. A Sonoscan C-SAM D9000 was used throughout the experimentation. In addition, the digital image analysis software (DIA) was used to obtain the percentage area of voiding of the underfill layer – this was one of the inputs to the predictive failure model. The parameters used for CSAM analysis are shown in Table 4-3.

Table 4-3 CSAM setup parameters

Parameter	Setting
Trigger	0.8
Frequency	230 MHz
Focal Length	0.5
Delay	21
Amplitude	49.5 dB

4.1.3 Summary of Assembly Specifications

There were two underfills used for the assembly of the test vehicles from Sections 4.1.1.1-4.1.1.4. The underfills were both no-flow fluxing underfills produced by the same manufacturer. To protect the identity of the supplier, the underfills will be referred

to as TL-Underfill C and TL-Underfill D. The material properties of these underfills are shown in Table 4-4.

Table 4-4 Underfill Material Properties

	TL-Underfill D	TL-Underfill C
T_g	88 °C	56 °C
Modulus > T_g	11MPa	11MPa
Modulus < T_g	1.6 GPa	2.4 Gpa
CTE < T_g	88 ppm/°C	71 ppm/°C
CTE > T_g	196 ppm/°C	196 ppm/°C
Poisson's ratio	0.3	0.3
Shear Modulus > T_g	4.23 MPa	4.23 MPa
Shear Modulus < T_g	.615 GPa	.923 GPa

The specifications for the assembly of all 3000 initial test vehicles are shown in Table 4-5. Recall, specifics about the process characterizations efforts leading to this build matrix were presented by Lazarakis [Lazarakis, 2003].

Table 4-5 Final Build Specifications for Test Vehicles 4.1.1.1-4.1.1.4

Test Vehicle	Underfill Material	Underfill Amount (mg)	Placment Force (N)	Dwell Time (s)	Reflow Profile	Number of Chips Assembled
FA10 2x2 Ni/Au	TL - Underfill C	9.0	1.0	0.5	Shown in Figure 3-1	170
FA10 2x2 Ni/Au	TL - Underfill D	9.0	1.0	0.5	Shown in Figure 3-1	170
FA10 2x2 OSP	TL - Underfill C	9.0	1.0	0.5	Shown in Figure 3-1	150
FA10 2x2 OSP	TL - Underfill D	9.0	1.0	0.5	Shown in Figure 3-1	150
FA10 4x4 Ni/Au	TL - Underfill C	21.0	3.0	1.0	Shown in Figure 3-1	170
FA10 4x4 Ni/Au	TL - Underfill D	21.0	3.0	1.0	Shown in Figure 3-1	190
FA10 4x4 OSP	TL - Underfill C	21.0	3.0	1.0	Shown in Figure 3-1	180
FA10 4x4 OSP	TL - Underfill D	21.0	3.0	1.0	Shown in Figure 3-1	150
FA10 2x2 Siemens	TL - Underfill C	9.0	1.0	0.5	Shown in Figure 3-1	100
FA10 2x2 Siemens	TL - Underfill D	9.0	1.0	0.5	Shown in Figure 3-1	100
PB6 2x2 Ni/Au	TL - Underfill C	8.5	1.0	0.5	Shown in Figure 3-1	216
PB6 2x2 Ni/Au	TL - Underfill D	8.5	1.0	0.5	Shown in Figure 3-1	228
PB6 2x2 OSP	TL - Underfill C	8.5	1.0	0.5	Shown in Figure 3-1	180
PB6 2x2 OSP	TL - Underfill D	8.5	1.0	0.5	Shown in Figure 3-1	150
PB8 2x2 Ni/Au	TL - Underfill C	8.0	1.0	0.5	Shown in Figure 3-1	150
PB8 2x2 Ni/Au	TL - Underfill D	8.0	1.0	0.5	Shown in Figure 3-1	150
Pb8 2x2 OSP	TL - Underfill C	8.0	1.0	0.5	Shown in Figure 3-1	150
Pb8 2x2 OSP	TL - Underfill D	8.0	1.0	0.5	Shown in Figure 3-1	150

4.2 FEM Modeling

Many of the predictive failure models that are currently available for solder fatigue in electronic packages are used in conjunction with Finite Element Modeling (FEM). As discussed in Chapter 2, many of these models are an empirical fit to data and are therefore rather application specific or material dependant. Finite element modeling was used as a ‘control’ methodology for predictive failure modeling.

4.2.1 Material Properties

Electronic packages are comprised of many different materials with very different material properties. Some of these materials can be modeled relatively accurately with a simple linear elastic model, while others need a more complex model. Solder, for example, is a very difficult material to model accurately with time-dependant as well as time independent behavior. The material models used throughout the finite element modeling effort will be discussed in this Chapter.

4.2.1.1 Silicon

Silicon was modeled as a linear elastic material [Tummala, 2001]. The material properties for Silicon are shown in Table 4-6.

Table 4-6 Material Properties of Silicon used for Finite Element Simulation [Tummala, 2001]

Silicon	
CTE	2.6×10^{-6} ppm/ $^{\circ}$ C
Modulus	1.6×10^5 MPa
Shear Modulus	6.5×10^4 MPa
Poisson's ratio	0.23

4.2.1.2 Underfill

Underfill is a polymer, specifically a thermosetting polymer, which has a glass transition temperature. A glass transition temperature is basically a temperature, actually a range of temperatures, where the material properties of the polymer change with the temperature of the material. It happens that the underfills used throughout the

experimental portion of the research had glass transition temperatures that were rather low which meant that the accelerated life testing conditions used temperature ranges that were higher than the T_g of the polymer underfill. The material properties of the underfill were entered into ANSYS as temperature dependant. The underfill material properties were provided by the underfill manufacturer and many of them were verified with dynamic mechanical analysis and thermal mechanical analysis. It was assumed that the change in material properties takes place over a 20 degree temperature change, so the temperature change chosen for the ANSYS simulation was ($T_g-10^\circ\text{C}$, $T_g + 10^\circ\text{C}$). The underfill material properties are shown in Table 4-7. The method of coding this in APDL is shown below Table 4-7.

Table 4-7 Underfill Material Properties for ANSYS Simulation

	TL-Underfill D	TL-Underfill C
T_g	88 °C	56 °C
Modulus > T_g	11MPa	11MPa
Modulus < T_g	1.6 GPa	2.4 Gpa
CTE < T_g	88 ppm/°C	71 ppm/°C
CTE > T_g	196 ppm/°C	196 ppm/°C
Poisson's ratio	0.3	0.3
Shear Modulus > T_g	4.23 MPa	4.23 MPa
Shear Modulus < T_g	.615 GPa	.923 GPa

So, for the TL-Underfill C material the ANSYS code that corresponds to this change in material properties is:

Table 4-8 APDL Code for Underfill Material Properties

APDL Code: Dimensions of FA10 2x2	Comments
	! TL - Underfill C w/ glass transition temperature of 329K)
	!Modulus values are in MPa, CTE values are in ppm/oC, temps in Kelvin
MPTEMP	!clears the temperature table
MPTEMP,1,248,319,339,398	!Defining a table of temperatures
MPDATA,EX,4,1,2.4E3,2.4E3,11,11	!Modulus in the x-direction
MPDATA,EY,4,1,2.4E3,2.4E3,11,11	!Modulus in the y-direction
MPDATA,EZ,4,1,2.4E3,2.4E3,11,11	!Modulus in the z-direction
MPDATA,ALPX,4,1,71E-6,71E-6,196E-6,196E-6	!CTE in the x-direction
MPDATA,ALPY,4,1,71E-6,71E-6,196E-6,196E-6	!CTE in the y-direction
MPDATA,ALPZ,4,1,71E-6,71E-6,196E-6,196E-6	!CTE in the z-direction
MPDATA,NUXZ,4,1,0.30,0.30,0.30,0.3	!poissons ratio xz
MPDATA,NUXY,4,1,0.30,0.30,0.30,0.3	!poissons ratio xy
MPDATA,NUYZ,4,1,0.30,0.30,0.30,0.3	!poissons ratio yz
MPDATA,GXZ,4,1,.923E3,0.923E3,4.23,4.23	!shear modulus xz
MPDATA,GXY,4,1,.923E3,0.923E3,4.23,4.23	!shear modulus xy
MPDATA,GYZ,4,1,.923E3,0.923E3,4.23,4.23	!shear modulus yz

Notice that the material properties were entered into ANSYS such that they could be easily changed to orthotropic if material properties were provided accordingly. Also, please note that there are four values for each of the material properties listed above; these correspond to the values for that given material property at the corresponding temperature in the MPTEMP command on the second line of the code.

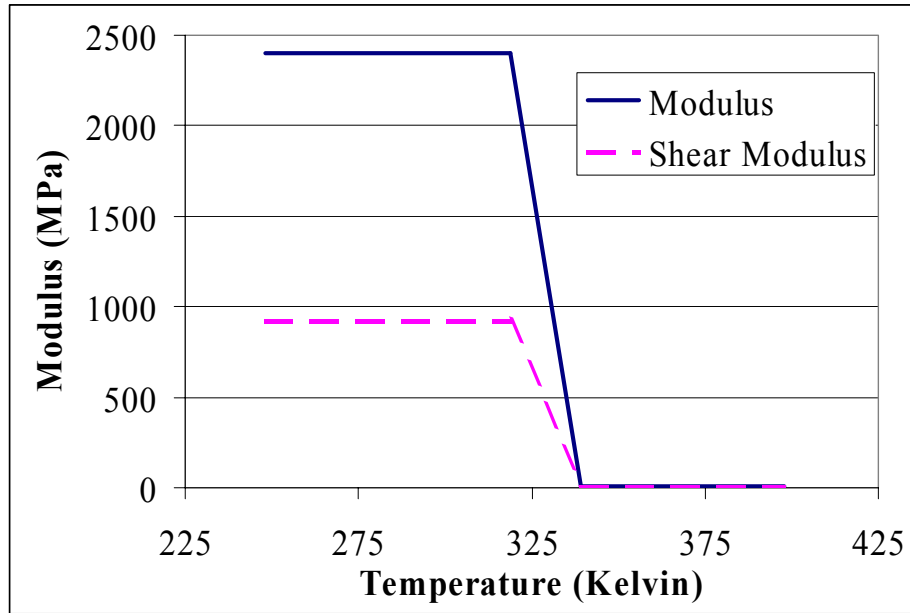


Figure 4-57 Shear Modulus and Young's Modulus as modeled with ANSYS: TL-Underfill C is used as an Example

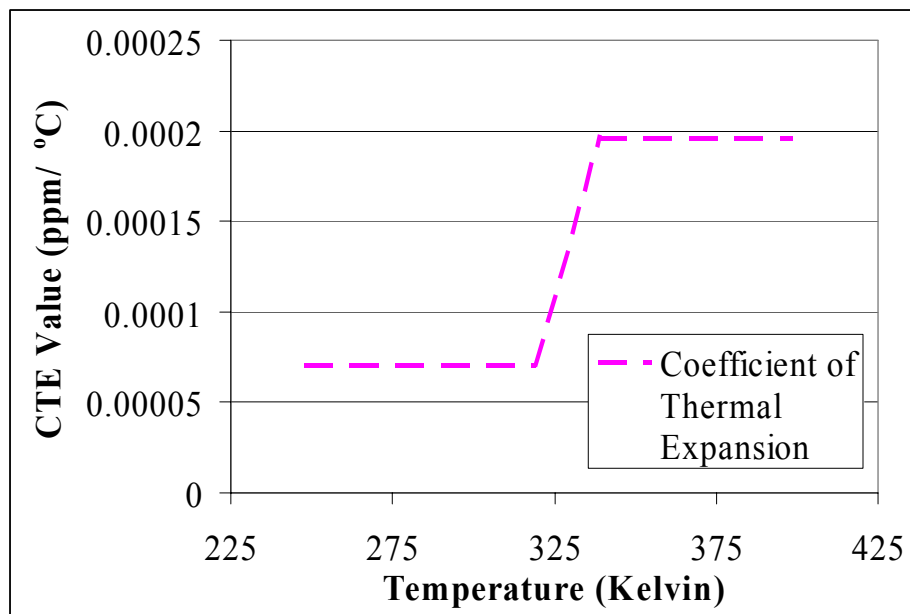


Figure 4-56 CTE as modeled with ANSYS: TL-Underfill C is used as an example

4.2.1.3 Underfill Properties as Measured with DMA and TMA

There are several tools available to evaluate the material properties of various polymers used for flip chip applications. Material characterization is important, mainly because without knowing the specific mechanical properties of a given underfill it would be difficult to decipher which underfill would be best for a given flip chip application. Important material properties are the coefficient of thermal expansion (CTE), the Modulus of elasticity (E), and the glass transition temperature (T_g). In addition, it is important to understand how the material properties of the underfill change with time and with thermal age, while they are being tested. To evaluate this, the TL-Underfill C material was tested at a post cure and post AATS. Since a large pan (with respect to the amount of underfill that is used in a flip chip assembly) of underfill was needed to prepare the samples for the DMA and TMA tests a pad of underfill was cured in an isothermal oven as opposed to sending the sample through the reflow oven.

A Thermomechanical Analyzer (TMA 2940 by TA Instruments) and a Dynamic Mechanical Analyzer (DMA 2980 by TA Instruments) were used to determine the Modulus, T_g , and CTE of the TL-Underfill C material post cure as well as after a 700 cycles air to air thermal shock (-55 to 125 °C). The TMA test basically uses the dimension change of the sample due to the applied thermal load as well as the temperature excursion to determine the coefficient of thermal expansion of a given material. The dynamic mechanical analyzer uses a cantilever sample with a fixed force at the end of the cantilever and measures the downward displacement of the cantilever sample to calculate the modulus of the material.

To prepare a test sample for both the DMA and TMA tests, underfill was cured in a small Aluminum pan where it was cured at 155 °C for one hour. A dicing saw was used to produce a small rectangular sample (approximately equal to 7.55mm x 1.58mm x 18.35mm) for the single cantilever DMA test, and a 5mm cube of underfill was used for the TMA test. The material property information is shown in the Table 4-9 for both the post cure and post-AATS TL-Underfill C samples.

Table 4-9 Table of DMA and TMA Results for TL-Underfill C

	Underfill C: Post Cure [165 °C for 1 hour]	Underfill C: Post AATS [700 cycles]
Modulus at 25°C	2223 MPa	2045 MPa
T_g	67.32 °C	72.42 °C
Modulus at T_g+40	15.00 MPa	14.00 MPa
CTE below T_g	96.20 µm/m°C	92.04 µm/m°C
CTE above T_g	201.0 µm/m°C	195.5 µm/m°C

There was not a significant change in the material properties of the underfill materials as they were thermally aged, as shown in Table 4-9. Therefore, for the purposes of finite element modeling, the material properties of the underfills were assumed to be constant throughout the accelerated life testing. The output of the DMA and TMA sample testing for underfill material C is shown in Figures 4-58 to 4-61.

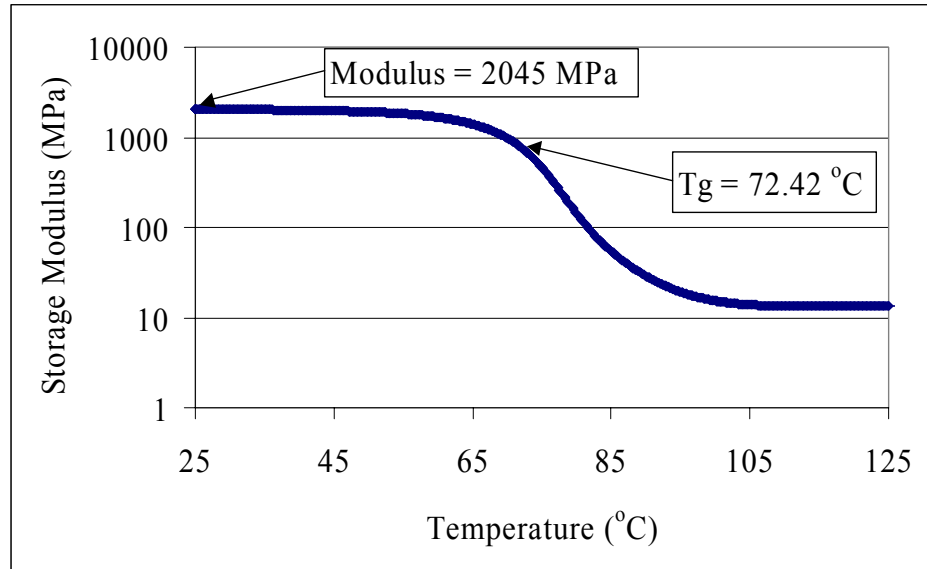


Figure 4-57 DMA Analysis Results for TL-Underfill C, Post AATS [700 cycles]

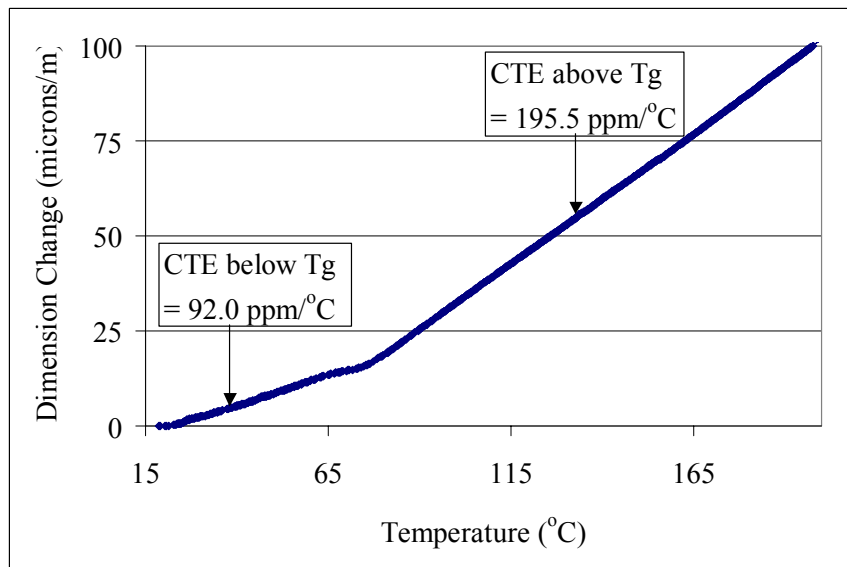


Figure 4-58 TMA Analysis Results for TL-Underfill C, Post AATS [700 cycles]

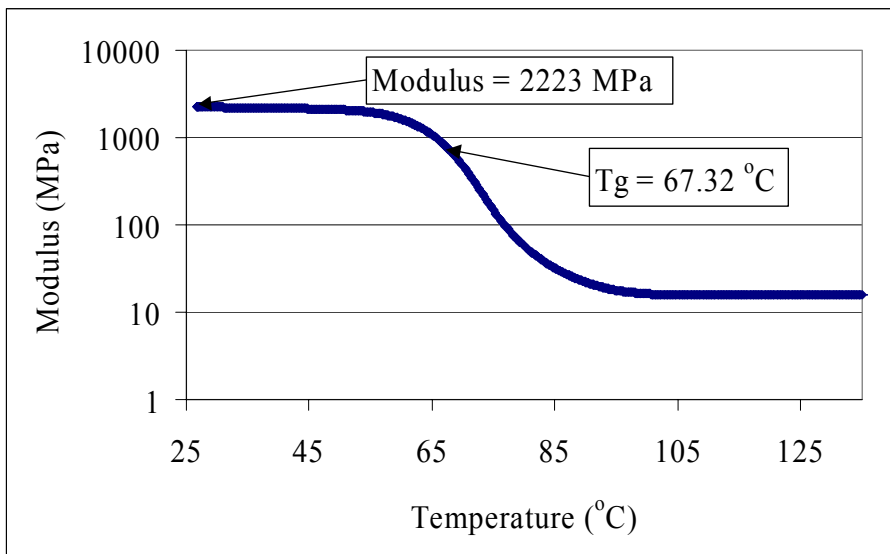


Figure 4-59 DMA Analysis Results for TL-Underfill C, Post Cure [155 °C for 1 hour]

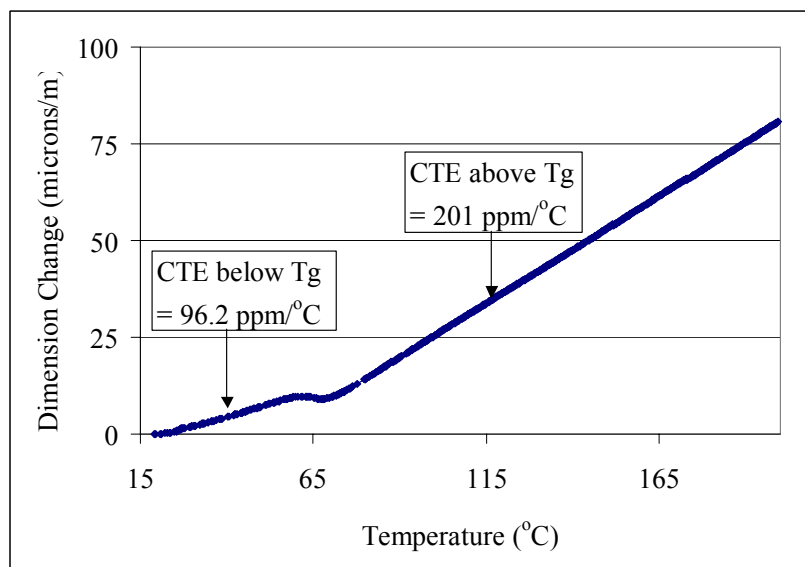


Figure 4-60 TMA Analysis Results for TL-Underfill C, Post Cure [155 °C for 1 hour]

4.2.1.4 Fire Retardant 4 (FR4) Substrate

The next material that was modeled was the FR4 substrate. The material properties for FR4 were temperature dependant [Barker 1993; Michaelides 1999]. The material properties used for the ANSYS simulation are shown in the Table 4-10.

Table 4-10 FR4 Material Properties for ANSYS Simulation [Michaelides, 1999]

	Temperature (in Kelvin)					
	303 K	368 K	383 K	398 K	423 K	543 K
Young's Modulus (x-direction)	22.4 GPa	20.68 GPa	19.97 GPa	19.30 GPa	17.92 GPa	16.00 GPa
Young's Modulus (y-direction)	22.4 GPa	20.68 GPa	19.97 GPa	19.30 GPa	17.92 GPa	16.00 GPa
Young's Modulus (z-direction)	1.60 GPa	1.20 GPa	1.10 GPa	1.00 GPa	0.60 GPa	0.45 GPa
Poisson's Ratio (xz)	0.1360	0.1360	0.1360	0.1360	0.1360	0.1360
Poisson's Ratio (xy)	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
Poisson's Ratio (yz)	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
CTE (x-direction)	20.0 ppm/°C	20.0 ppm/°C	20.0 ppm/°C	20.0 ppm/°C	20.0 ppm/°C	20.0 ppm/°C
CTE (y-direction)	86.5 ppm/°C	86.5 ppm/°C	243 ppm/°C	400 ppm/°C	400 ppm/°C	400 ppm/°C
CTE (z-direction)	20.0 ppm/°C	20.0 ppm/°C	20.0 ppm/°C	20.0 ppm/°C	20.0 ppm/°C	20.0 ppm/°C
Shear Modulus (xz-direction)	630 MPa	600 MPa	550 MPa	500 MPa	450 MPa	441 MPa
Shear Modulus (xy-direction)	199 MPa	189 MPa	173 MPa	157 MPa	142 MPa	139.3 MPa
Shear Modulus (yz-direction)	199 MPa	189 MPa	173 MPa	157 MPa	142 MPa	139.3 MPa

This data was used for the modeling of all FR4 substrates. A TMA and DMA analysis was performed on the high T_g substrates used in the experimental portion of this project. This analysis could only give information about the coefficient of thermal expansion, CTE, in the thickness dimension because of the way that the TMA test is conducted. The substrates are thin, ~ 0.78 mm, such that they cannot be supported correctly to acquire a dimension change in the x and y direction. The modulus of the substrates, E , was acquired as well as the glass transition temperature, T_g , via TMA analysis. The results are shown in Figures 4-62. Notice that the glass transition temperature of the substrates was lower than the expected value of 180 °C; which was supplied by the circuit board manufacturer. The difference in glass transition temperatures does not matter for the

purposes of the FEM simulation because the glass transition temperature was never exceeded during the accelerated life tests that were performed. Therefore, there was no need to enter temperature dependant properties into ANSYS.

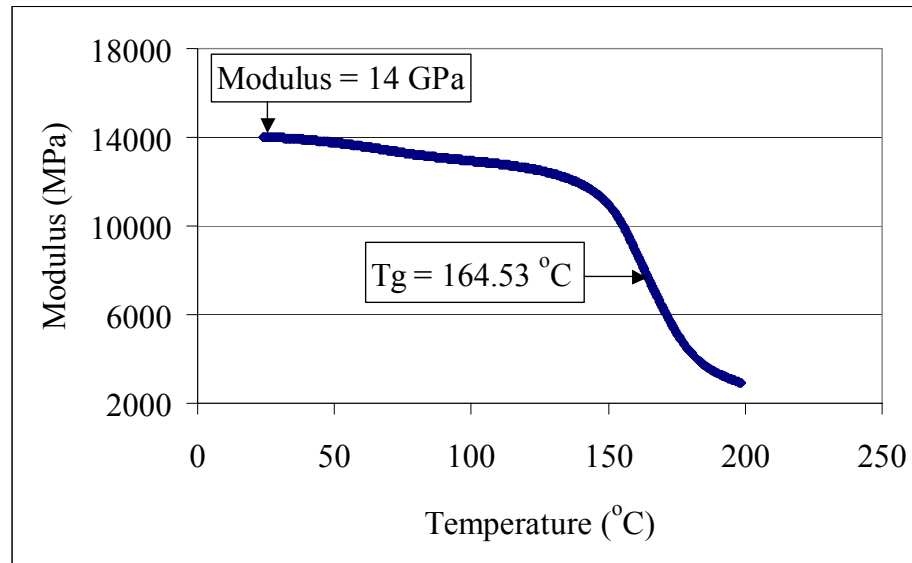


Figure 4-61 DMA Analysis Results for high T_g FR4 substrates, Post Cure [155 °C for 1 hour]

4.2.1.5 Solder

Solder was modeled using a rather complex material model. Solder is a complicated material to model, mainly because it exhibits time dependent as well as time independent behavior at the operating temperature ranges. The melting point of eutectic (63Sn/37Pb) solder is 183°C, therefore creep (time dependent inelastic deformation) must be considered for fatigue of solder in the range from -55°C to 125°C.

The 63Sn/37Pb solder material was modeled with a Elastic-Plastic-Creep Model. The Elastic-Plastic portion of the material behavior was modeled using multi-linear

kinematic hardening. Five different stress and strain values were input into ANSYS for 4 different temperatures. The strain rate for the data listed in the table below was 0.0081/sec [SRC/CINDAS 1995]. This meant that any of the strain based fatigue predictive failure models could be used in conjunction with the output of the model to calculate a number of cycles to failure. On the other hand, if Anand's model was used the total inelastic strain would be output. This saves computational time, but the creep strain and the time-independent plastic strain cannot be extracted for ANSYS independently, which limits the reliability models that one can use.

Table 4-11 Multi-Linear Kinematic Hardening of 63Sn/37Pb Solder for ANSYS Model

Strain	Stress (MPa) @ 248K	Stress (MPa) @ 298K	Stress (MPa) @ 358K	Stress (MPa) @ 398K
0.001	27.39	19.65	15.27	11.68
0.002	41.36	29.68	22.51	16.12
0.003	47.93	34.12	26	18.56
0.004	50.3	36.35	27.83	19.88
0.005	50.77	37.24	28.64	20.55

To capture the effects of time-dependant inelastic deformation power law creep was used [Ju *et al.*, 1994]. The paper by Ju *et al* provides the constants for the equation:

$$\dot{\epsilon}_s = A \sigma^n e^{-\left(\frac{Q}{RgT}\right)} \quad (4-1)$$

Note that the subscript 's' stands for steady state creep rate. The constants are in Table 4-12:

Table 4-12 Creep Constants used in ANSYS Model for Solder [Ju *et al.*, 1994]

A	$1.84 \times 10^{-4} (\text{MPa})^{-n} (\text{s})^{-1}$
n	5.2
Q	50 kJ/mol
R_g	$8.314 \times 10^{-3} \text{ kJ/K-mol}$

4.2.2 Geometry

The geometry used for the ANSYS simulation was 2D using plane strain. There were a total of 3 different geometries modeled: FA10 2x2, FA10 4x4, PB8 4x4. The geometry was generated with a bottom-up approach, starting first with key points, then, lines, areas, etc. The geometries generated in ANSYS are shown in Figures 4-63 to Figure 4-65.

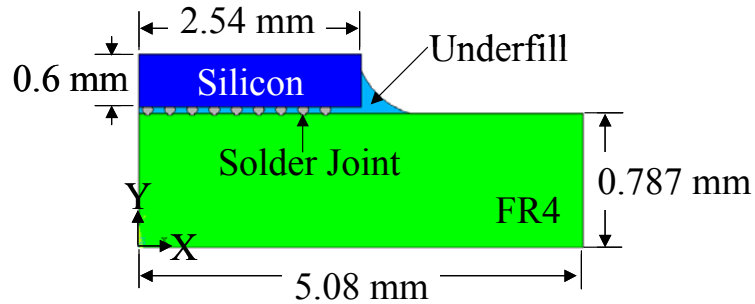


Figure 4-62 FA10 2x2 Geometry

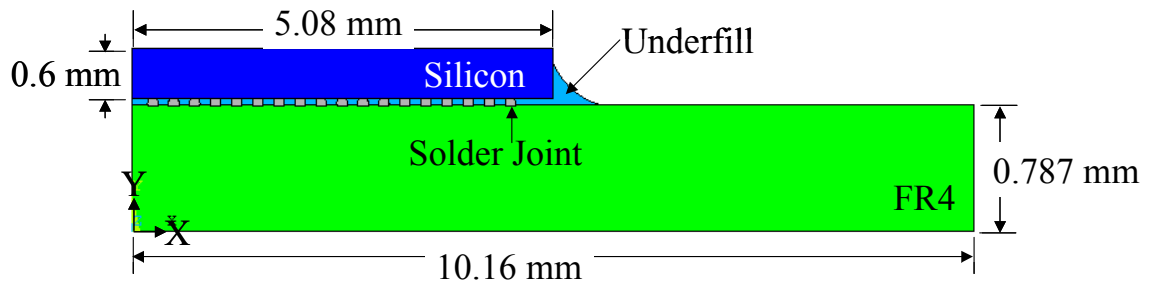


Figure 4-63 FA10 4x4 Geometry

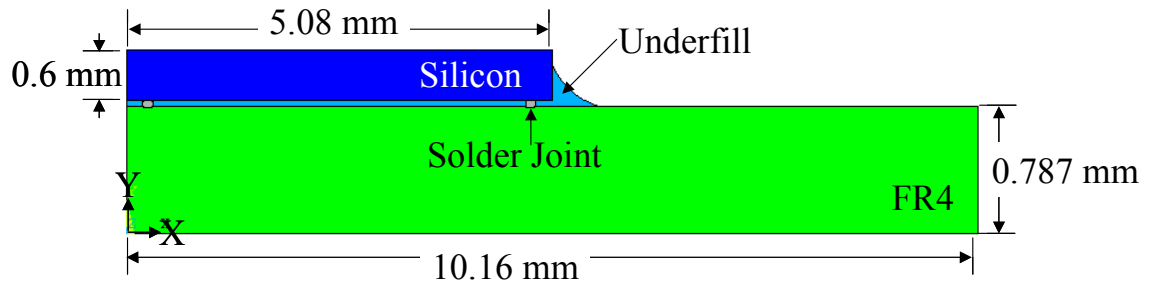


Figure 4-64 PB8 4x4 Geometry

The geometries were programmed into ANSYS using APDL or ANSYS Parametric Design Language. The other option would be to model the geometries using the GUI, graphical user interface. The GUI can be cumbersome to program in mainly because there is no ‘undo’ command and mistakes can often require the programmer to start over at the last saved file. APDL code is written as a text file and read into the software using the file → read input from... option on the main menu of ANSYS 7.0. APDL is easy to learn and it allows for easy manipulation of the input geometry and material properties, for example, it is very easy to modify the mask opening to change the wettable substrate pad area or to modify the modulus of the underfill. There were several important inputs that defined the geometry of the various flip chip on board component level packages. The ANSYS APDL code below shows the critical dimensions for the FA10 2x2 geometry.

Table 4-13 APDL code for Dimensions of a FA10 2x2 Test Vehicle

APDL Code: Dimensions of FA10 2x2	Comments
bump_r = .06	!bump diameter of 120 microns
ubm_r = .051	!UBM diameter of 102 microns
pad_r = .025	!radius of wettable pad area
pitch = .203	!pitch of bumps
fc_thk = .600	!flip chip thickness
fr4_thk = 1.5	!fr4 board thickness
stnd_off = .095	!stand off
die = 2.54	!die size, 2x2inches
fillet= .8*fc_thk+stnd_off	!u-fill fillet radius-approximate with arc
mask = .015	!soldermask thickness
bump_x = .076	!firstbump x location
bump_y = 2.346	!all bumps y location
bump_z = -0.5*stnd_off	!all bumps z location

Please note that the full APDL code is in Appendix A. Notice that the dimensions can be easily changed and the simulation can be re-ran, this is why APDL code was used to model the various component level packages. Overall dimensions for the 3 packages are shown in Table 4-14.

Table 4-14 Table of Flip Chip on Board Package Dimensions used in ANSYS Simulation

	FA10 4x4	FA10 2x2	PB8 4x4
Flip Chip Bump Radius	0.06 mm	0.06 mm	0.06 mm
UBM Radius	0.051 mm	0.051 mm	0.051 mm
Substrate Mask Opening Radius	0.051 mm	0.051 mm	0.052 mm
Flip Chip Bump Pitch	0.254 mm	0.254 mm	0.203 mm
Thickness of the Flip Chip	0.6 mm	0.6 mm	0.6 mm
Thickness of the PCB	0.7874 mm	0.7874 mm	0.7874 mm
Standoff Height	0.095 mm	0.095 mm	0.09095 mm
Overall Size of the Die	10.16 mm x 10.16 mm	5.08 mm x 5.08 mm	10.16 mm x 10.16 mm
Mack Height	0.015 mm	0.015 mm	0.010 mm
# of I/O	1268	317	352
# of Bumps in FEM Simulation	18	9	2

4.2.3 2D Plane Strain

Figure 4-66 shown the 2D plane strain geometry of a component level package. These are the boundary conditions applied to all of the 2D plane strain models. The 2D models that were generated used 2D elements with 2 degrees of freedom for each of the nodes in the finite elements. The assumption of plane strain basically means that the components of strain in the z direction are zero ($\epsilon_{zz}=0$, $\epsilon_{xz}=0$, $\epsilon_{yz}=0$). This assumption is valid along the center of an area array package that is much wider than it is thick. The packages are symmetric about the center line and therefore only half of the package needs to be modeled. This symmetric condition is shown in Figure 4-66. All boundary conditions were applied at the nodes of the meshed geometry; to prevent any motion of the package, there is a rigid body constraint at the bottom-center node, due to the symmetry of the package the geometry is constrained from movement in the x-direction as shown in Figure 4-66.

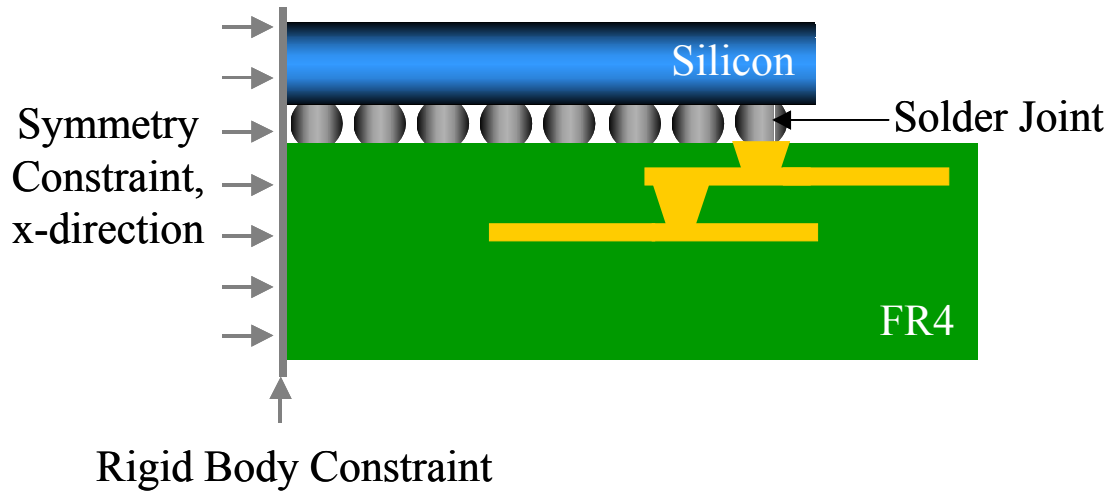


Figure 4-65 2D Geometry Showing Boundary Conditions: Rigid Body Constraint and Constraint to Account for No Movement at Neutral Point

4.2.4 Element types chosen for the 2D Model

The element type used for the 2D models was PLANE82 for solder, and PLANE2 for underfill, silicon, and FR4. PLANE2 is a six node triangular element. PLANE2 has quadratic displacement behavior and is well suited to model irregular meshes. The element is defined by six nodes having two degrees of freedom at each node: translations in the nodal x and y directions. PLANE2 can be used as a plane element (plane stress or plane strain) or as an axisymmetric element. The element also has plasticity, creep, swelling, stress stiffening, large deflection, and large strain capabilities. The PLANE2 element type, shown in Figure 4-67, is compatible with the 8-node PLANE82 element, shown in Figure 4-68, which was used to model solder. PLANE82 provides more accurate results for mixed (quadrilateral-triangular) automatic meshes and can tolerate irregular shapes without as much loss of accuracy. The 8-node elements have compatible displacement shapes and are well suited to model curved boundaries; this is good for the solder joint shape since the joints are barrel shaped. PLANE82 is defined by eight nodes having two degrees of freedom at each node: translations in the nodal x and y directions. The element may be used as a plane element or as an axisymmetric element. The element has plasticity, creep, swelling, stress stiffening, large deflection, and large strain capabilities.

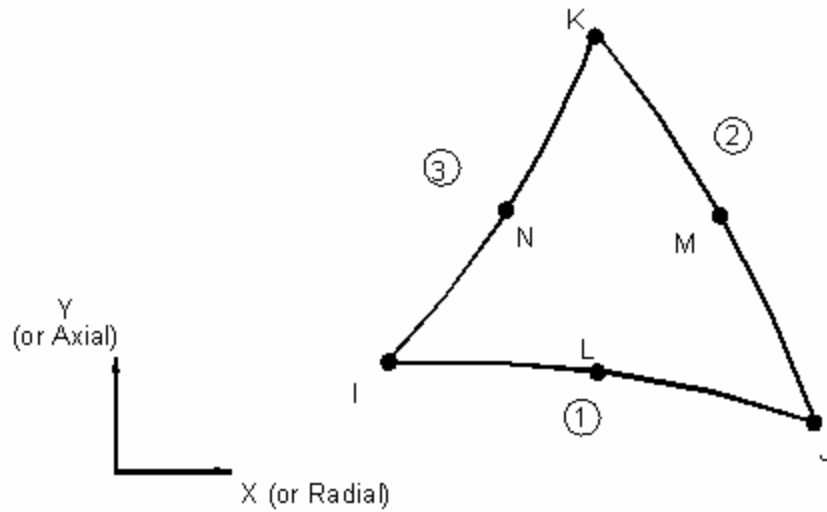


Figure 4-66 PLANE2 Element [ANSYS Theory Manual] used to model Underfill, Silicon, and FR4: a 6-node element

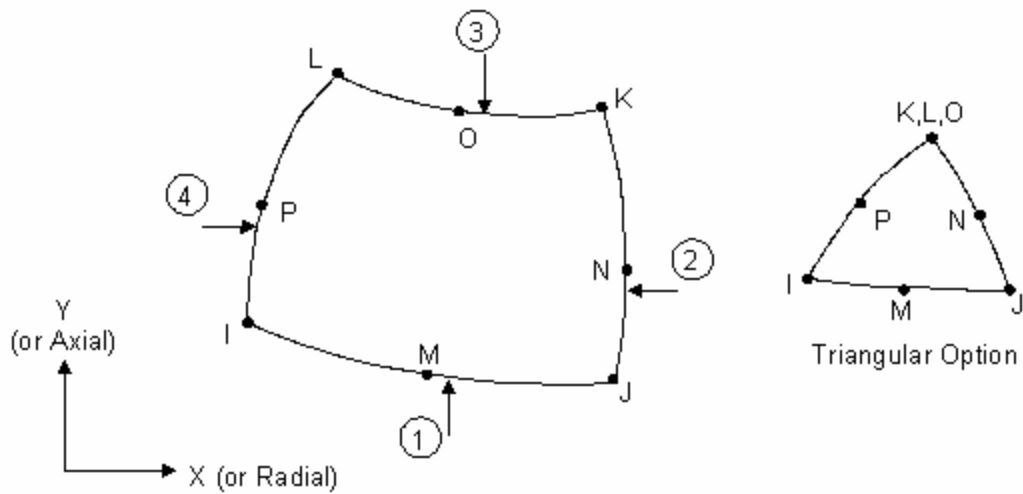


Figure 4-67 PLANE82 Element [ANSYS Theory Manual] used to model Solder: an 8-node element

A picture of the resulting meshed geometry is shown in Figure 4-69 for the FA10 2x2. Please note that FA10 2x2 geometry was meshed with the free mesh option, the size

of the mesh was controlled by altering the line segments via the LESIZE command in ANSYS APDL code.

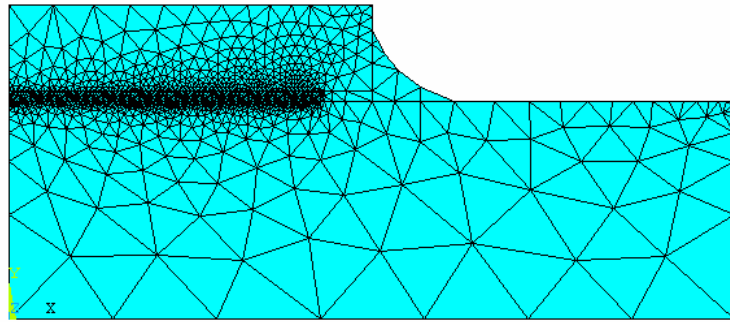


Figure 4-68 Meshed FA10 2x2 with PLANE2 and PLANE82 Elements

4.2.5 Post Processing work in ANSYS

There are many ways to convert the output from a finite element package into a life time prediction, the method listed in this section is a general method that can be used for flip chip on board component level assemblies. The fundamental premise in this modeling methodology is that the electronic components experience low cycle fatigue ($N_f < 10^5$ cycles) such that strain based fatigue equations can be utilized to predict cycles to failure. The inelastic strain that is experienced in the solder joint is entered into a Coffin-Manson type relationship (or if more than one relationship is necessary, the effective total damage to the solder is quantified via Miner's rule). Depending on the predictive equation and the methods in which the constants were developed for that equation, the output might be the mean time to failure or the time to first failure. The method detailed in the following sections will predict the mean time to failure of the components (MTTF).

4.2.5.1 Acquiring Strain Values

The total von Mises stress and strain were acquired for all nodes in given regions of the solder joint. The von Mises strain was calculated independently for the creep and time-independent plastic strain components; this was necessary because the predictive failure models that were used required them to be independent.

To calculate the strain in the various regions of the solder joint an area averaging was used, where the average of the nodal creep strain values over several elements was calculated for each load step. For example, the elements in the upper left region of the solder joint were selected as the first region (Figure 4-73). The element numbers that compose Region 1 are: 109, 123, 97, and 124. To select these elements the following APDL code was used:

```
esel,s,elem,,123,124      !Region#1
esel,a,elem,,97
esel,a,elem,,109
eplo t
```

Once these specific elements were selected the nodal values of stress and strain were tabulated for only these elements. The menu path that is used to acquire a list of these values is: General post-processing, List Results, Nodal Solution, click stress, click components (EPCRCOMP), click OK. This will output the component values of stress as each node and the effective stress at each node in the selected region, for a single load step. This data is collected for all load steps. The same process is used for calculating both the creep strain and the plastic strain. The average of the effective stress and strain at the end of each load step are then determined in Excel; this procedure will be covered in Section 4.2.5.2.

The effective stress and strain are then plotted, that graph is shown in Figure 4-71. Notice that there are a total of three cycles plotted in the graph and each of the cycles is a different color. The resulting stress strain behavior, in Figure 4-71, is typical of what one would expect for tin-lead solder. There is a fair amount of time dependent inelastic deformation at the hot side of the thermal cycle and there is minimal inelastic deformation at the cold side of the cycle. The solder experiences creep at the hot side of the cycle where it is at $.68T_{\text{melt}}$. It should be noted that the same calculations were performed for other regions of the solder joint, and the region of the solder joint with the highest stress/strain values was used in the predictive equations because that is the region that would drive fatigue failure in the solder joint. It should be noted that the strain calculations were not very sensitive to element size in this model, simply because an average of strain over several elements was used. The strain at a single node should never be used to predict cyclic fatigue failure because strain at a node does not converge.

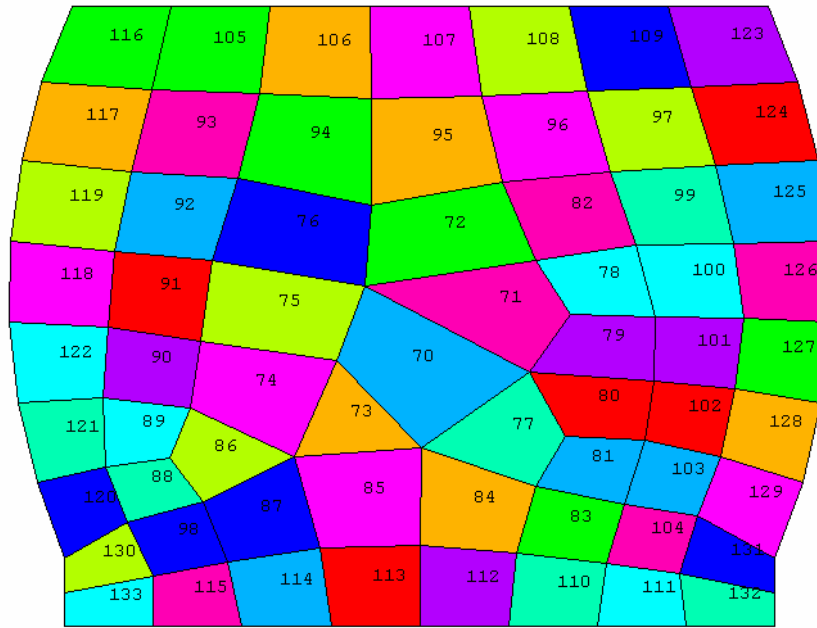


Figure 4-69 Schematic of Element numbers in the Solder Joint

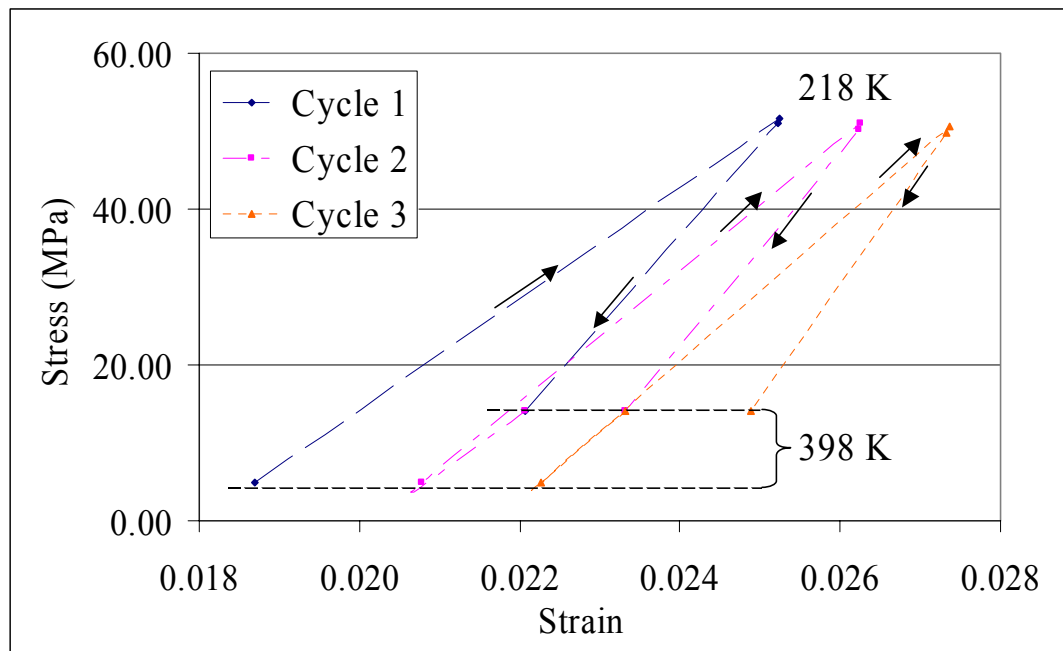


Figure 4-70 Typical Cyclic Stress Strain Behavior of Solder in the FE Model

Notice the accumulated strain that is induced during each thermal cycle, in addition to the stress relaxation. This behavior is expected of solder, in addition there is creep strain at the high side of the thermal cycle (this is shown in the graph at the hot side of the thermal cycle (398K), it occurs between the dashed lines in Figure 4-71). Also, please note that the stress free temperature of the assembly was 183 °C, 456K, so the assembly does not return to a zero-stress state while it is cycling. The next step in the post processing process is to calculate the cycles to failure.

4.2.5.2 Determining the Cycles to Failure

There are several strain-based models that are available for the prediction of cycles to failure. A combination of the Cutiongco model and the Knecht & Fox were used with Miner's rule to determine the cycles to failure; this method was chosen based on the work presented by Pyland [Pyland, 2002]. For these models the plastic and creep strain were necessary for one total thermal cycle. The models require an equivalent strain from a thermal cycle, thus the von Mises strain was calculated. In general, the von Mises strain can be calculated using the following equation:

$$\epsilon_{eff,i} = \frac{1}{\sqrt{2(1+\nu')}} \left[(\epsilon_{x,i} - \epsilon_{y,i})^2 + (\epsilon_{y,i} - \epsilon_{z,i})^2 + (\epsilon_{x,i} - \epsilon_{z,i})^2 + \frac{3}{2} \left((\epsilon_{xy,i})^2 + (\epsilon_{yz,i})^2 + (\epsilon_{xz,i})^2 \right) \right]^{1/2} \quad (4-2)$$

Where the normal and shear strains are $\epsilon_{x,i}$ $\epsilon_{y,i}$ $\epsilon_{z,i}$ and $\epsilon_{xy,i}$ $\epsilon_{yz,i}$ $\epsilon_{xz,i}$ respectively and ν' is the effective poisson's ratio. Since the inelastic (creep and plastic) strains are desired for the purposes of using the Cutiongco and Knecht & Fox models a poisson ratio

of 0.5 was used which makes the equation above (hence, the 'NE' superscript means not elastic):

$$\varepsilon_{eff,i}^{NE} = \frac{\sqrt{2}}{3} \left[(\varepsilon_{x,i}^{NE} - \varepsilon_{y,i}^{NE})^2 + (\varepsilon_{y,i}^{NE} - \varepsilon_{z,i}^{NE})^2 + (\varepsilon_{x,i}^{NE} - \varepsilon_{z,i}^{NE})^2 + \frac{3}{2} \left((\varepsilon_{xy,i}^{NE})^2 + (\varepsilon_{yz,i}^{NE})^2 + (\varepsilon_{xz,i}^{NE})^2 \right) \right]^{1/2} \quad (4-3)$$

An effective, or von Mises, strain was calculated for both the time dependant and time independent plastic deformation of the solder. To calculate the creep and plastic strain independently the following menu path was used: General post proc→List results→Nodal Solution→Strain-Creep (for plastic strain select 'Strain-Plastic') →Comp's EPCRCOMP→OK. Once the values were obtained for each of the individual load steps that make up a thermal cycle the maximum effective inelastic strain was determined for each of the cycles. A cycle is defined as a soak in both the hot and the cold chambers in addition to the transition ramps between thermal chambers. The –40 to 125 °C cycle shown in Figure 4-72, shows the ramp down from the stress free temperature of 183 °C to room temperature and then a total of three complete thermal cycles. ANSYS™ outputs only the final strain information at the end of each of the load steps; notice that a total of four load steps make up a single thermal cycle.

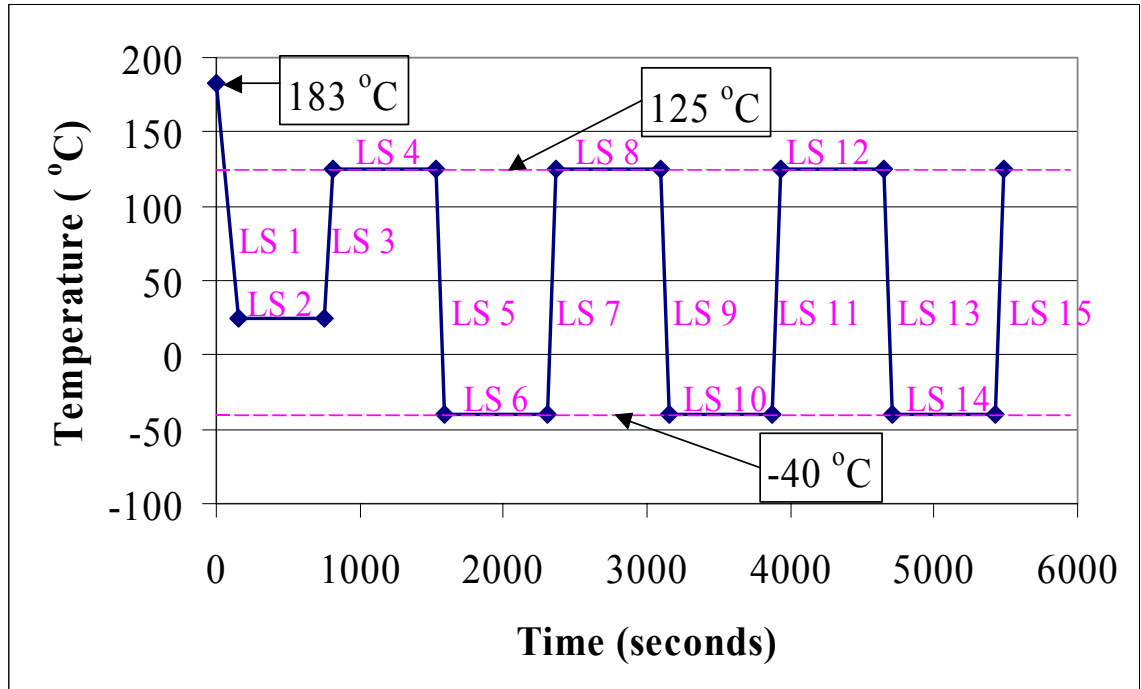


Figure 4-71 Thermal Shock profile for FEM simulation [-40 to 125 °C ;12 min dwells]:

The Load Steps (LS) are labeled

To determine the inelastic strain in a cycle only nodes in the critical areas of the solder joints were selected. The nodes in the top and bottom corners of the solder joint were highlighted and the cycles to failure for each of these critical regions was determined and the lowest value of cycles to failure was chosen as the final output of the modeling effort. This is because this is the region of the solder joint that is expected to fail first and drive fatigue failure of the solder joint in thermal cycle. The various regions of the solder joint that were investigated are shown in Figure 4-73.

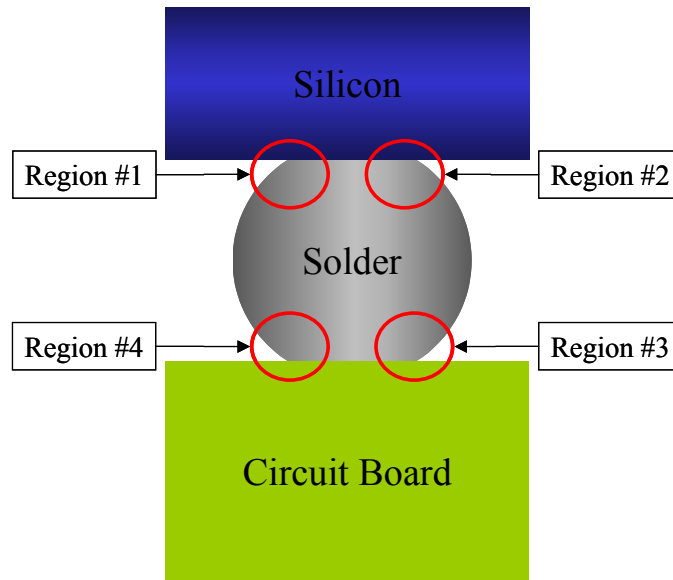


Figure 4-72 Diagram of Solder Joint Regions Used to Determine Fatigue Performance with FEM

An averaging of strain values was used to minimize the effects of any geometric singularities in the solder joint. An average of the strain values over 4 elements, and 16 nodes was used to determine the strain in the regions described in Figure 4-73 above. An example of the calculation for a single load step is shown in Table 4-15.

Table 4-15 Plastic Strain Calculation for a Single Load Step in a Single Region of the Solder Joint

Plastic Strain Over a Single Load Step					
Load Step 11	node #	strain x	strain y	strain z	strain xy
	1511	0.0140	-0.0161	0.0021	-0.0341
	1513	0.0253	-0.0266	0.0013	0.0286
	1515	0.0116	-0.0140	0.0024	0.0230
	1532	0.0018	-0.0038	0.0020	0.0003
	1534	0.0039	-0.0061	0.0021	-0.0017
	1631	0.0073	-0.0093	0.0020	0.0101
	1640	0.0124	-0.0144	0.0020	0.0169
	1649	0.0068	-0.0083	0.0015	0.0065
	1664	0.0045	-0.0061	0.0015	0.0017
		0.0097	-0.0116	0.0019	0.0057

This analysis was conducted for plastic as well as creep strain for each of the load steps that makes up the thermal cycle and each of the four regions of the solder joint. The maximum difference in inelastic strain (creep or plastic for any given region of the solder joint) between the loads steps that make a cycle is used in the prediction equations. The creep shear strain range was used in conjunction with the Knecht & Fox equation with a C=1.7 [Knecht, 1991].

$$N_f = \frac{C}{\Delta\gamma_{mc}}, \text{ in cycles} \quad (4-4)$$

Note that the shear strain values that are output from ANSYS™ need to be multiplied by $\sqrt{3}$ to get the appropriate value for shear strain for the Knecht & Fox equation: this is because the Knecht & Fox equation only requires the *creep shear strain range* NOT the *equivalent creep shear strain range*.

The von Mises plastic strain range was input into the Cutiongco equation with C equal to 1.919 and n equal to -1.35 [Cutiongco, 1992].

$$N_f = C\Delta\epsilon_p^n, \text{ in cycles} \quad (4-5)$$

Now that the effects of the plastic and creep strain have been used with appropriate models their relative effect on low cycle fatigue can be determined using the Palmgren-Miner Rule [Dowling, 1993].

$$\frac{1}{N_f} = \frac{1}{N_{f(mc)}} + \frac{1}{N_{f(p)}} \quad (4-6)$$

The fatigue life of the solder due to creep strain only is calculated using the Knecht & Fox equation and the fatigue life of solder due to time independent, or plastic, strain is determined using the Cutiongco model, these effects are then combined using Miner's rule to generate a fatigue life prediction of the solder joint. This methodology is used for all FEM solder joint life prediction equations in this thesis.

5 MODELING

In this chapter, there are a total of three predictive failure models presented; a statistics based model, an analytical model, and a correction factor approach. All of these models are for the prediction of cycles to failure due to low cycle fatigue; these models are specifically looking at the mean time to failure and not the rate at which failure occurs. To capture a rate effect several sets of data would need to be generated with various shape and scale parameters for the Weibull distribution, the shape could then be used as a predictor of reliability performance. The same regression techniques that are described in Appendix B could be used to fit a shape parameter as a predictor of performance.

Finite element modeling methods used to assess reliability performance were outlined in the previous chapter. The finite element modeling work was conducted mainly as a ‘control’ for the modeling effort, this allowed for a comparison with basic predictive modeling methods that are widely used and accepted throughout the electronics industry. The details of the various modeling methods were discussed in this chapter; however a brief summary of the models were presented to outline the modeling effort.

The statistics based model was presented to illustrate how regression techniques could be used to determine a predictive failure model for a flip chip on board application [Muncy, 2003].

$$N_f = 81.45(2.62)^{\ln(1+f)} (1.72)^M \left[\frac{A_{UBM}}{A_{Pad}} \right]^{-1.38} \left[\frac{\alpha_{UF} (T_g - T_{Min})}{\Delta\alpha (T_{max} - T_g)} \right]^{0.16} \quad (5-1)$$

A shortcoming with the model in Equation 5-1 is there is no term for the plastic strain range for a single thermal cycle as would be expected for a strain based fatigue equation. Recall, that the empirical strain-life relationship proposed by Coffin-Manson [Manson & Coffin 1965, 1954] relates the total number of cycles to failure to the plastic strain range. For fatigue of solder joints the Coffin-Manson equation can be written as a function of the inelastic shear strain range, $\Delta\gamma$, given by:

$$N_f = \frac{1}{2} \left(\frac{\Delta\gamma}{2\varepsilon'_f} \right)^{1/c} \quad (5-2)$$

Where N_f is the cycles to fatigue failure. ε'_f is the fatigue ductility coefficient and c is the fatigue ductility exponent, these represent the fatigue characteristics of a given material.

To accommodate this shortcoming an analytical model was proposed to calculate the total inelastic shear strain range of a solder joint through one thermal cycle. The plastic strain range for a single thermal cycle was calculated from an equation developed by Zhang (Equation 5-3) and the creep shear strain was calculated via a single power law creep (Equation 5-5).

A model for the time-independent plastic shear strain range was proposed by Zhang [Zhang, 2003].

$$\gamma_p(x) = \frac{\alpha_2^{xy} (\Delta T_2 - \Delta T_1)x + \frac{h_2}{3G_2} [\tau_2(x) - \tau_1(x)] + \frac{h_2 x}{\rho(x)}}{h_2 \left[1 + \alpha_2^z \left(\frac{\Delta T_1 + \Delta T_2}{2} \right) \right]} \quad (5-3)$$

Please note that this is a modified version of the popular model developed by Suhir for bi-metal thermostats [Suhir, 1986]. The plastic strain range as calculated by Equation 5-3

was used in conjunction with Soloman's model to determine the number of cycles to failure due to plastic strain [Soloman,1987].

$$N_f = C\Delta\gamma_p^n \quad (5-4)$$

Soloman's model was for 60/40 solder, and fatigue was defined as the number of cycles to halve the load range required to produce plastic strain. The constants for this model were developed for solder under simple shear testing conditions. This equation was based on the plastic shear strain range. For the temperature range of -50°C to 125°C the constants C and n are 1.29 and -1.96 respectively. The time-dependant inelastic (creep) behavior of solder was modeled via a single power law creep relation.

$$\dot{\epsilon}_s = A\sigma^n e^{-\left(\frac{Q}{R_g T}\right)} \quad (5-5)$$

Note that the subscript 's' stands for steady state creep rate. Values for the constants were published by Ju [Ju *et al.*, 1994], these were detailed in Table 4-12. A and n represent experimentally determined material constants, Q represents the activation energy for creep, R_g represents the universal gas constant, T is the temperature of the solder in Kelvin, and σ is the current stress state. The stress values for the creep expression, σ , were determined from the analytical model presented in Equation 5-3. The total creep strain at the high and the low temperatures in thermal cycle were obtained by integrating the expression in Equation 5-5 over the time in the thermal zone. The difference in the creep strain between the hot and the cold zones provides the creep shear strain range over one thermal cycle. The value for the creep shear strain range was then used in conjunction with the Knecht & Fox equation with a $C=1.7$ [Knecht, 1991].

$$N_f = \frac{C}{\Delta\gamma_{mc}} \quad (5-6)$$

The effects of creep and plastic strain generate a variable amplitude loading on the solder joint material. Therefore the effects of both of these loads were combined using the Palmgren-Miner Rule [Dowling, 1993].

$$\frac{1}{N_f} = \frac{1}{N_{f(mc)}} + \frac{1}{N_{f(p)}} \quad (5-7)$$

This result provided a prediction of cycles to failure by a simple analytical method. The next step in the modeling effort was to assign correction factors for variables that could not be modeled with a simple analytical approach. Regression techniques, much the same as those that were used to generate the model in Equation 5-1, were again used to fit a model that would generate correction factors for (1) solder joint shape; (2) the glass transition temperature of the underfill material; and (3) the metallization of the substrate bond pads. The model was presented in two general forms first as a correction to an unmodified fatigue life prediction (Equation 5-8) and then as a basic strain based fatigue equation (Equation 5-9) similar to the one presented by Coffin-Manson.

$$N_f = C_{\text{metallization}}(\text{Pad finish}) \cdot C_{\text{joint shape}}(A_{\text{UBM}}, A_{\text{Pad}}) \cdot C_{T_g}(\text{Underfill}) \cdot N_f' \quad (5-8)$$

$$N_f = C_{\text{metallization}}(\text{Pad finish}) \cdot C_{\text{joint shape}}(A_{\text{UBM}}, A_{\text{Pad}}) \cdot C_{T_g}(\text{Underfill}) \cdot \Delta\gamma_p^{-1.29} \quad (5-9)$$

Specific values and relationships for the correction factors were presented in the last section of this chapter. A detailed step by step regression analysis was presented in Appendix B; this outlines the steps taken to arrive at the final correction factors. A general discussion will be presented in this chapter.

5.1 Statistics Based Methodology for Developing Predictive Failure Models for Component Level Assemblies

This section presents a methodology for assessing the reliability performance of electronic components. A reliability prediction equation was developed for a flip chip on board assembly to illustrate the method. The model was intended for the prediction of mean time to failure, measured in cycles, in thermal cycle or thermal shock. This methodology allowed for the incorporation of non-traditional predictors of performance such as the glass transition temperature of the underfill material, the metallization of the substrate bond pads and the non-dimensional quantity of UBM area to the wettable substrate bond pad area. The predictors of reliability performance will be different for various package types; however the method of assessing the relative importance of the various predictors will be the same. Regression techniques were used to determine the best predictors for reliability performance. The strongest predictors were incorporated into the predictive failure model.

5.1.1 Introduction to Predictive Model Development

Environmental stress tests, or accelerated life tests, apply stresses to electronic packages that exceed the stress levels experienced in the field. In theory, these elevated stress levels generate the same failure mechanisms that are seen in the field, only at an accelerated rate. The reliability engineer then determines how the accelerated life testing data should be used (or extrapolated) to determine how the component would perform during field operating conditions. The methods of assessing reliability performance of

electronic packages could be classified into two categories: statistics based approaches and physics of failure based approaches. Statistics based approaches assume that a mathematical relationship exists between the accelerated life testing data and the actual field performance of the device, so the failure rate obtained in a lab environment could then extrapolated to a use condition [Veshnfsky, 1999]. Most physics of failure based approaches focus on the fatigue of solder joints. The most common mechanism of failure, solder fatigue, is either fully or partially responsible for 90% of all mechanical and electrical failures [Tummala, 2001].

A multitude of publications provide low cycle strain based fatigue equations that could be used as cyclic life predictors [Engelmaier, 1984; Pecht, 1997; Soloman, 1986; Knecht & Fox, 1991; Hong, 1997; Lau 1997; Darveaux, 1997], many of these low cycle strain based fatigue equations were presented in Chapter 2. These equations were based on the original low cycle strain based fatigue equation for metals presented by Coffin & Manson [Coffin, 1954; Manson, 1965]. Although these models could be very useful in predicting the relative performance of solder joints in different electronic packages they were not as good at predicting the absolute number of cycles to failure for a given component structure. Said another way, there exists a fundamental disconnect between the predictions made by these models and the actual performance of components in reliability testing. The methodology presented in this Chapter could be used to better understand some of the physics of failure associated with various failure mechanisms and to incorporate additional predictors of performance to enhance the prediction capabilities of many of the Coffin-Manson models currently available in the literature.

In this chapter, a statistics based methodology was used to identify the critical factors in reliability performance of a component level assembly; where the critical factors under investigation were determined via a physics of failure approach in combination with experimental observations. The relative influence of critical factors on reliability performance was determined via statistical regression techniques. This methodology incorporated regression analysis results into the constants for the predictive life equation. The end product was a general lifetime prediction equation rather than one that was specific to a certain test vehicle or material set. To illustrate the method, a flip chip on board component level assembly was investigated; however, this same methodology could be used to evaluate various other component level package assemblies. The first step in the model generation process was to determine which input variables would be good predictors of reliability performance; this started with the examination of a large set of experimental data. To generate this data, approximately 1200 test vehicles were subjected to thermo-mechanical fatigue conditions in accelerated life testing: air-to-air thermal cycling (AATC) and liquid-to-liquid thermal shock (LLTS). The test vehicles incorporate four different test die, eight board configurations, two no-flow underfill materials, and two substrate metallizations. These test vehicles were described in detail in Sections 4.1.1.1-4.1.1.4. It should be mentioned that many manufacturers of electronic components would already have this data available, and would simply be able to run this statistics based analysis on previously obtained failure data. For the purposes of this modeling effort a solid failure database was necessary and therefore experimental accelerated life testing was the first step in the model generation effort. It should be mentioned that the final strain based model with correction factors

presented in Sections 5.2.5.1 and 5.2.5.2 used failure data from test vehicles described in Sections 4.1.1.1 through 4.1.1.11. The detailed step by step procedure was presented in Appendix B.

5.1.2 Experimental

The first step in the predictive failure model development was to determine what input parameters should be included in the statistical regression analysis. To determine which parameters were needed a large sample set of flip chip on board test vehicles were assembled and subjected to accelerated life tests. The samples used for this experimental data set were described in Sections 4.1.1.1-4.1.1.4. The air-to-air testing was completed by J. Muncy and the liquid-to-liquid data was obtained by T. Lazarakis. The AATC data was detailed in Section 6.1.1, the LLTS data was detailed by Lazarakis [Lazarakis, 2003].

5.1.2.1 Materials

There were a total of sixteen independent test vehicles used throughout the study; all test vehicles were described in Sections 4.1.1.1 -4.1.1.4. These test vehicles incorporated 4 different test die, eight substrates, and two non-commercially available underfills. The Silicon die used were standard test die provided by Flip Chip Technologies, both area array and peripheral array devices were evaluated. In addition, 5mm and 10mm size test die were evaluated. The eight substrates used in the testing were provided by several sources and incorporated two different bond pad metallizations.

Lastly, the underfill used was a no-flow fluxing underfill that did not contain filler particles. The underfills used in this experimental work were TL-Underfill C and TL-Underfill D.

5.1.2.2 Assembly Process

The process used for the assembly of the test vehicles in the study consisted of a Cam-a-Lot 3700 underfill dispensing machine, a Siemens F5 IC placement machine, and a BTU paragon reflow oven with seven independent thermal zones. Specifics about the processes used for the assembly of the test vehicles are found in Chapter 2. Several design of experiments were run to determine the process windows for the aforementioned assembly equipment. The concern during the process characterization was not only yield, but also to determine how some of the processing decisions impacted reliability performance of the component level assemblies. So, in addition to yield, reliability performance was used as an evaluation parameter throughout the process characterization effort. Again, please refer to Chapter 2 for more details on the assembly parameters.

The underfill process, the flip chip placement process, and the reflow process were characterized prior to the final assembly of test vehicles that were used in this analysis. In the underfill dispense process characterization the amount of underfill dispensed and the dispense pattern were investigated. The selected dispense process used a dispense of 9 mg of underfill for the 10mm die and 5 mg of underfill for the 5mm die. A dot dispense pattern resulted in the lowest percentage of voiding and the best reliability performance. The next process characterized was die placement. The die was placed

with a SIPLACE Siemens F5 placement machine with a downward force of 5 N. The dip module fluxing parameters were a dwell time of 1 second and a startup of 5 for the 10mm die. Once the die was placed the test vehicle was passed through a thermal profile in a BTU Paragon seven zone reflow oven where the solder interconnects formed and the thermosetting underfill polymer cross linked. The reflow profile is shown in Figure 4-55. The amount of cross linking was chosen as one of the evaluation parameters for the design of experiments in addition to thermal shock reliability performance. A picture of an assembled FA10 4x4 test vehicle is shown in Figure 5-1. The actual test board was a 10-up design; only one site was shown in the figure below. The small square pads surrounding the die were electrical probing pads that allowed for electrical continuity testing of different sections of the die so the location of a solder joint failure could be determined.

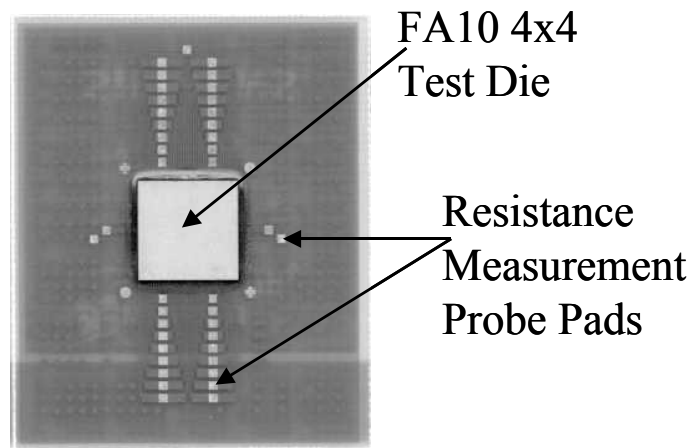


Figure 5-1 Picture of Assembled Substrate

5.1.2.3 Reliability Testing

Samples were tested in air-to-air thermal cycle condition B (AATC) according to standard JESD22-A104-B and liquid-to-liquid thermal shock condition C (LLTS)

according to standard JESD22-A106-A; all samples were removed from test every 100 cycles to inspect for interconnect failures. The integrity of the solder joints was investigated by a simple electrical continuity test, where an increase in resistance of 10% from the original daisy chain resistance value was classified as a failure and the component was removed from testing.

5.1.2.4 Failure Mode Analysis

The test vehicles used throughout the experimental portion of this project were a 10-up or a 12-up configuration, meaning that each test board had 10 or 12 individual flip chip assemblies. Once a component failed electrical continuity testing, it had to be removed from the test board to allow the remainder of the flip chip assemblies to continue testing. Some of the test vehicles incorporated breakaways allowing for removal of an individual component during testing. In other test vehicles, individual components were separated from the substrate with a high speed cutting tool. It was important to remove components from test at the interval when they failed, simply because the failure mode that caused the electrical failure needed to be identified.

To determine the mode of failure for each test vehicle several failure mode analysis techniques were used. X-ray imaging was used to look for underfill cracks and solder extrusion, C-mode Scanning Acoustic Microscopy (CSAM) was used to determine if there had been any delamination between the die and the underfill or die cracking, cross sectioning and scanning electron microscopy (SEM) were used to investigate

fatigue cracks in the solder, and finally EDX analysis was used to evaluate material concentrations.

There were three main modes of failure found in the test vehicles subjected to liquid-to-liquid thermal shock and air-to-air thermal cycle. The failure modes were: die cracking, solder extrusion into underfill voids, and solder fatigue cracks. Figure 5-2 shows an SEM image of solder extrusion into an underfill void. The void initially encompassed the gap between the two flip chip bumps, allowing a path for the solder to extrude.

The second failure was die cracking, approximately 1% of the die showed some level of die cracking at post reflow optical inspection.

The third mode of failure was fatigue cracking of the solder joints. This is the mode of failure that was focused on for the purposes of the model presented in this thesis. Figure 5-3 shows a typical fatigue crack found via cross section and SEM analysis. The crack starts in the top right corner of the bump continues into the solder joint and across the diameter of the bump.

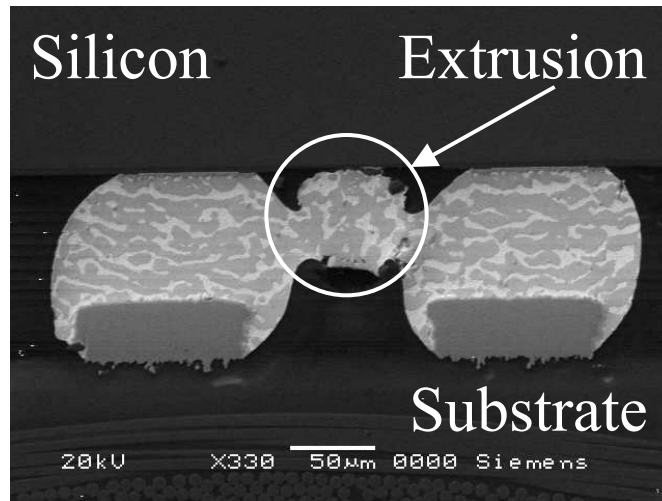


Figure 5-2 SEM image of solder extrusion into underfill void

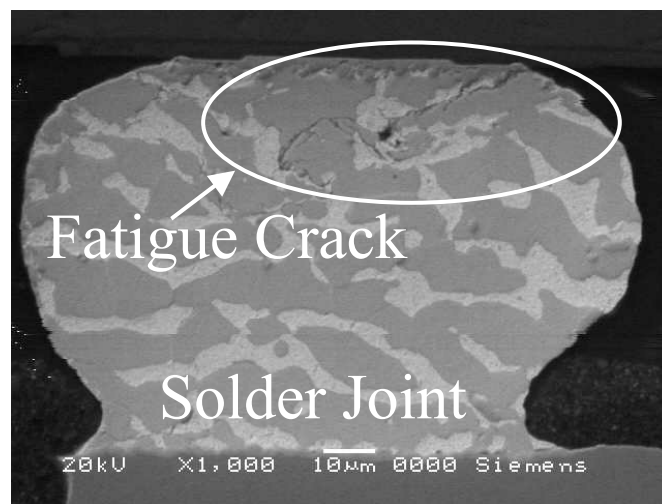


Figure 5-3 Fatigue Crack of Flip Chip Bump

5.1.3 Methodology for Predictive Failure Model Development

Once a large sample set of experimental data was obtained a regression analysis technique was used to determine which input parameters had an influence on the reliability performance of the components in accelerated life testing. The input

parameters investigated varied with the component package type. For the case of a flip chip on board component level assembly, the input parameters investigated were substrate metallization, substrate mask opening area versus the UBM area of the flip chip bump, die size, perimeter or full area array flip chip interconnect pattern, underfill material properties, location of the die on the test board, frequency of cycling, number of I/O, and percent area voiding. The percent area voiding was measured post-reflow on the Sonoscan CSAM series D-9000, using Visual Acoustics digital image analysis software.

Two regression analysis techniques were investigated using MinitabTM software version 13.32: a multiple linear regression and a regression with life data. The latter analysis technique allowed for arbitrarily censored treatment of the failure data, meaning that the interval failure data as well as right censored failure data could be used. Multiple linear regression was the method used to determine the final coefficients, refer to Appendix B for details. A general flow diagram of the methods used in selecting predictors is shown below:

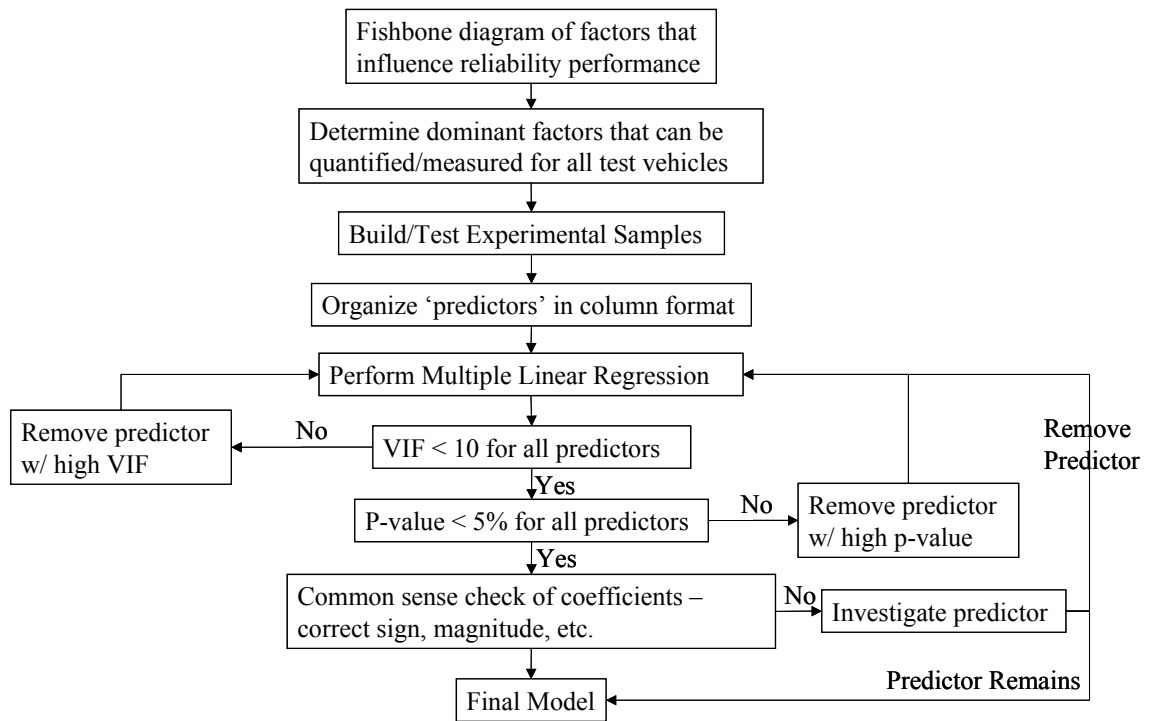


Figure 5-4 General Flow Diagram for Predictor Selection

As a first attempt in investigating the relative importance of the various input parameters a multiple linear regression was conducted. The MinitabTM session output listed in Table 5-1 was divided into different sections, so that each of the sections could be discussed in turn. The output of the regression analysis was linear as the name multiple *linear* regression would imply. Each of the input predictors was given a coefficient as shown in the second line of the MinitabTM output in Section I of Table 5-1. Multiple linear regression was used because it allowed the response variable, MTTF, to be modeled as a linear function of more than one input variable.

$$y_i = \beta_o + \beta_1 x_{1i} + \cdots + \beta_k x_{ki} + e_i \quad (5-10)$$

The coefficients $\beta_o, \beta_1, \dots, \beta_k$ were unknown parameters and they were estimated by the method of least squares. In general terms, the least squares fit minimized the sum of

squared deviations between the experimental data observations and their fitted values. The output of the regression analysis which was the first line of the Minitab™ output in Section I of Table 5-1 was:

$$\begin{aligned}
 MTTF = & 1713 + 10.8(\text{percentage of underfill voiding}) + 1.02(\text{Component \#}) + \dots \\
 & - 0.0356(\text{Number of I/O}) - 73719(\text{average wettable pad area}) - 826(P/A \text{ die}) + \dots \quad (5-11) \\
 & - 369(\text{substrate metallization})
 \end{aligned}$$

The second part of Section I listed the various input parameters, or predictors, and their corresponding p-values. A p-value that was less than 5% indicated that there was sufficient evidence to suggest that the coefficient of the input parameter was non-zero meaning it should be considered in the formulation of the predictive failure model. In the flip chip on board example, the predictors such as component number on the circuit board, the number of I/O, and the underfill voiding percentage should be removed from the prediction effort. These predictors were removed because the p-values for component number, the number of I/O, and the voiding percentage were .764, .458, and 0.083, respectively; this was well above the cutoff threshold p-value of .05. The predictors should be removed from the regression model one at a time as p-values will change once a predictor has been removed. The last part of Section I is the R-Squared statistic, or coefficient of determination, which was a diagnostic used to assess the ‘fit’ of the model. The model, as presented in Equation 5-11, explained 73.4% of the variability in the MTTF of the 1160 components that were investigated. Larger values of R-squared tend to indicate that the data points are closer to the fitted regression line, however a lower R-squared value does not necessarily mean that the model was not appropriate, a fitted regression line may be accurate and informative even if the R-squared value was low.

The p-value shown in Section II of the MinitabTM session window is 0.0, this means that the chosen input parameters, or predictors, in some way affect the output. If the p-value in this section was high that would mean that all input parameters chosen were not good predictors (i.e. start over and choose some different predictors).

The third section of the MinitabTM output lists any points that were outliers as well as those that have a very high leverage (marked with an X in the st. resid column), a high leverage point had a strong influence in the fit of the model and the resulting coefficient. These points should be scrutinized to make sure that they were: (a) correct such that there was not a clerical error and (b) that they were not due to some experimental anomaly, in which case, it would be worth re-running the model without this point to see how the model changes.

Table 5-1 Session Window Output from Minitab™ Multiple Linear Regression Analysis

Section I: Regression Equation				
MTTF = 1713 + 10.8 (Voiding percentage) + 1.02 (Component #) - 0.0356 (Number of I/O) - 73719 (Average Pad Area) - 826(Area or Perimeter Array Die) - 369(Metallization)				
Predictor	Coefficient	SE Coefficient	T	P-Value
Constant	1713	138.5	12.37	0.000
Voiding %	10.836	6.219	1.74	0.083
Component #	1.017	3.377	0.3	0.764
Number of I/O	-0.03556	0.04783	-0.74	0.458
Wettable Pad Area	-73719	10776	-6.84	0.000
Area or Perimeter Die	-826.08	85.76	-9.63	0.000
Substrate Metallization	-368.81	25.4	-14.52	0.000
	S = 164.3	R-Sq = 73.4%	R-Sq(adj) = 72.7%	

Section II: Analysis of Variance					
Source	DF	SS	MS	F	P-Value
Regression	6	16857519	2809587	104.13	0.000
Residual Error	226	6097760	26981		

Section III: Unusual Observations						
Observation Number	Percentage of Underfill Voiding	Cycle Component Failed at	Fit	SE Fit	Residual	St Resid
31	19.7	700	1114.8	65.3	-414.8	-2.75RX
37	18.3	900	1100.5	57.4	-200.5	-1.30 X
45	17.2	1100	1091	52.5	9	0.06 X
51	6.9	1300	975.5	30.1	324.5	2.01R
60	9.8	1400	1002.9	26.3	397.1	2.45R
61	9.7	1400	1003.8	24.2	396.2	2.44R
62	9.9	1400	1012.1	28.3	387.9	2.40R
63	9.3	1900	999.5	24.4	900.5	5.54R
230	2.9	900	572.6	31.8	327.4	2.03R

With a multiple linear regression analysis completed, the relationship between the various input parameters and the output, MTTF, for a various test vehicles was known.

Recall that this regression analysis was run on 1160 experimental data points encompassing 2 underfills, 8 circuit boards, and two substrate metallizations. Although this is interesting, it is not a very good model, mainly because the fatigue of solder and failure of components in general is not usually a linear relationship. To further this modeling effort, information about the physics of failure of various components and the mathematical relationship between the input parameters and the MTTF of the component was needed. Again, this model was developed with multiple linear regression and the relationship between the inputs and the output MTTF was linear. If the relationship is non-linear the inputs to the regression analysis must be manipulated such that they can be used in multiple linear regression.

This makes more sense in the context of the flip chip on board example. For example, several researchers have investigated the effects of solder joint shape on reliability performance (in addition, it was investigated via finite element modeling in later sections of this thesis) so this would be a good example of the type of predictor that is needed in a model for flip chip on board reliability prediction. To quantify the effect of solder joint shape a non-dimensional parameter was developed; the area of the under bump metallurgy over the area of the substrate pad, $A_{UBM}/A_{SUBSTRATE_PAD}$.

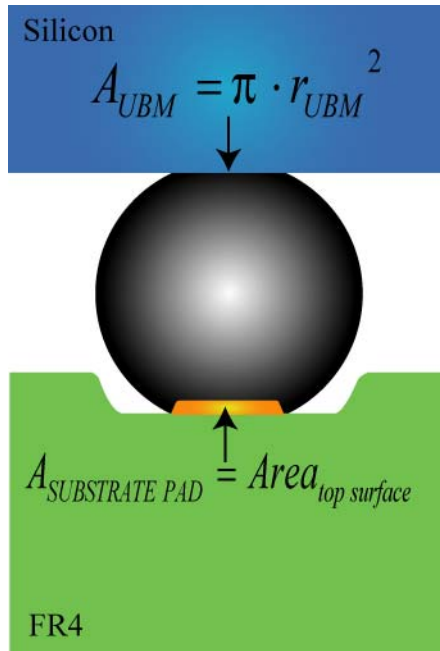


Figure 5-5 Definition of the solder joint shape areas for regression model

Notice that this was one of the terms in the final model that was developed for the flip chip on board component level structure (Equation 5-1). More about specific terms will be outlined later in this section; the next step is to discuss why the final model does not look linear when a multiple linear regression was used to develop the model. The model was not linear, but it was intrinsically linear, meaning that it could be converted to a linear form and analyzed with multiple linear regression. A simple example will be used to illustrate this; assume that the following equation describes the MTTF for a given component:

$$MTTF = \gamma_o e^{\gamma_1 x} \quad (5-12)$$

which could also be expressed as

$$\ln MTTF = \ln \gamma_o + \gamma_1 x \quad (5-13)$$

Where,

$$output = \ln MTTF$$

$$\beta_o = \ln \gamma_o$$

$$\beta_1 x = \gamma_1 x$$

For simple linear regression the equation:

$$output = \beta_o + \beta_1 x \tag{5-14}$$

This shows how the inputs could be mathematically manipulated such that simple linear regression or multiple linear regression techniques could be used to generate more complex failure models, provided the final model was intrinsically linear. If the final model was not intrinsically linear, non-linear regression techniques would be needed. SAS JMP statistical discovery software provides non-linear regression functions, however this will not be discussed in this thesis.

5.1.4 Regression Analysis

A total of approximately 1160 data points from both liquid-to-liquid thermal shock and air-to-air thermal cycle were evaluated via statistical regression techniques. The regression analysis techniques discussed in general terms in Section 5.1.3 were applied to the experimental data set of 1160 flip chip on board assemblies to produce a predictive failure model. Regression analysis was used to determine which input parameters helped to predict the reliability performance of the flip chip solder joints in air-to-air thermal cycle and liquid-to-liquid thermal shock. Some of the input variables that were initially chosen were highly correlated, for example, die size and the number of flip chip bumps. Therefore, these input variables needed to be removed from the

regression analysis simply because their presence was redundant. The final session window output for the regression model was shown in Table 5-2.

Table 5-2 Minitab Session window output for regression analysis

Section I: Regression Equation				
$\ln(\text{cycles to failure}) = 4.40 + 0.169\text{metallization}*(\ln 25) - 1.38 \ln(\text{UBM/sub}) + 0.159 \ln(\text{CTE term}) + 0.299 \ln 25^{(\ln(1+f))}$				
Predictor	Coefficient	SE Coefficient	T	P-Value
Constant	4.3976	0.1392	31.59	0.000
Metallization* ln(25)	0.16936	0.01203	14.08	0.000
ln(UBM area/ wetable pad area)	-1.38395	0.055	-25.16	0.000
ln(strain term)	0.15943	0.02469	6.46	0.000
ln25^(ln(1+f))	0.29868	0.02143	13.94	0.000
	S = .6220	R-Sq = 52.1%	R-Sq(adj) = 51.9%	

Section II: Analysis of Variance					
Source	DF	SS	MS	F	P-Value
Regression	4	434.87	108.72	281.04	0.000
Residual Error	1034	399.99	0.39		

Section III: Unusual Observations						
Observation Number	Percentage of Underfill Voiding	Cycle Component Failed at	Fit	SE Fit	Residual	St Resid
48	3.22	4.6052	7.2299	0.0425	-2.6247	-4.23R
232	3.22	4.6052	7.2299	0.0425	-2.6247	-4.23R
601	0	7.3778	6.1241	0.0446	1.2537	2.02R
602	0	7.4384	6.1241	0.0446	1.3143	2.12R
.
.
.
954	3.22	5.2983	6.9084	0.0391	-1.6101	-2.59R
955	3.22	5.2983	6.9084	0.0391	-1.6101	-2.59R
967	3.22	5.2983	6.9084	0.0391	-1.6101	-2.59R

The input variables that resulted in p-values that were below 5% remained in the model, inputs with higher p-values were removed. Variables that generated high p-values were die size, number of I/O and underfill voiding percentage. It should be noted that more inputs will always mathematically make the R-squared value increase. However, the utility of the predictive model would not be enhanced with these added inputs, quite the contrary, the equation would then become cumbersome to use, with too many inputs. The final predictive model given in Equation 5-1 is restated below. The regression output was simplified mathematically; removal of the natural log generated a model where the terms were multiplicative.

$$N_f = 81.45(2.62)^{\ln(1+f)} (1.72)^M \left[\frac{A_{UBM}}{A_{Pad}} \right]^{-1.38} \left[\frac{\alpha_{UF} (T_g - T_{Min})}{\Delta\alpha(T_{max} - T_g)} \right]^{0.16} \quad (5-15)$$

All model parameters are listed in Table 5-3.

Table 5-3 Parameters for the Reliability Model

Variable	Description
N_f	Mean Time to Failure (MTTF) [cycles]
M - Metallization	Cu/OSP - Enter 1
	Cu/Ni/Au - Enter 0
f	Frequency of cycles per hour [cph]
A_{UBM}	Area of the Under Bump Metallurgy
A_{Pad}	Wettable pad area
T_g	Glass transition temperature of the underfill
T_{min}	Minimum temperature in thermal cycle test
T_{max}	Maximum temperature in thermal cycle test
α_{UF}	Coefficient of thermal expansion (CTE) of the underfill
$\Delta\alpha$	CTE difference between Si and FR4

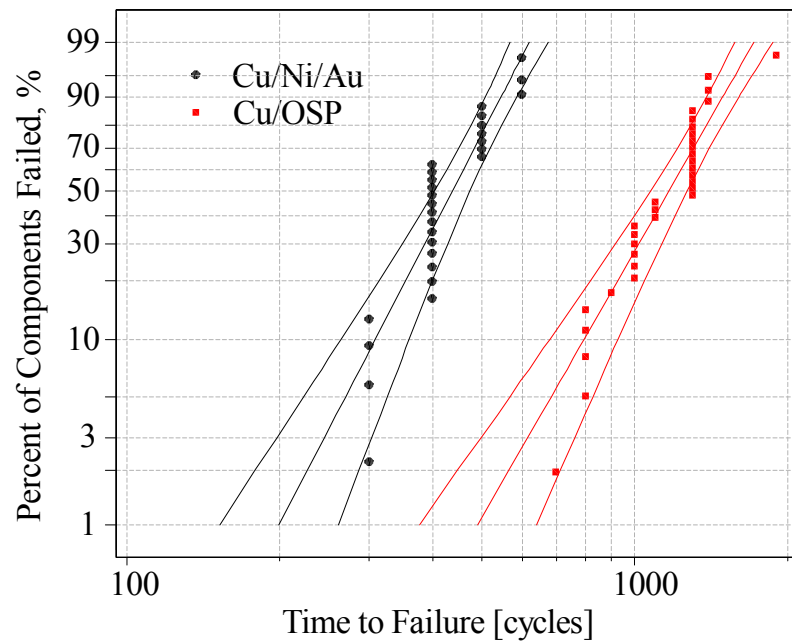


Figure 5-6 Probability Plot, FA104x4 with TL-Underfill C; reliability performance shift between Cu/Ni/Au and Cu/OSP substrate metallization (shown with a 95% CI)

One interesting input to the reliability prediction equation was the metallization of the substrate bond pads, ‘M’ in the model. The probability plot for the 10mm full area array die shows a marked shift in performance between the Cu/Ni/Au and the Cu/OSP substrate metallizations (Figure 5-6). This shift in performance was experienced for both underfills and all board/die configurations. Through EDX analysis it was found that there was approximately 2.8 wt% gold detectible after assembly and thermal cycling. The Au from the Cu/Ni/Au substrate pads was evenly distributed throughout the solder bump as revealed by an element mapping. The brittle intermetallic AuSn_4 forms when the gold content in a tin/lead solder joint is above 0.33 wt% [Massalski, 1987]. It is believed that the shear strength of the solder slowly decreases with increasing gold concentration

above the critical limit of 0.33 wt% [Duan, 2003]. Lastly, above 3 wt% of Au the bulk solder becomes brittle and weak as a result of the excess intermetallic AuSn_4 platelets in the solder volume [Harper, 1997]. The solder joints failed in the bulk of the solder under the intermetallic formed at the UBM side of the solder joint, but the cracks did not appear to originate in the intermetallic layer. It should be noted that the flip chips used throughout this study had an Al/Ni/Cu under bump metallurgy.

Additionally, there is a term to account for the flip chip solder joint shape. The solder joint shape was quantified by the ratio of the area of the UBM area to the wettable substrate bond pad area. The frequency term is used to account for the shift in number of cycles to failure that occurs as a result of increased damage in the solder experienced in longer isothermal dwells due to reduced frequency of thermal cycles.

Finally, there is a strain term. This term is used to account for the thermally induced strain experienced by the solder joints as a result of thermo-mechanical loading. This is not the actual strain that the solder joints experience, it is however, constructed such that it is a strong predictor of cycles to failure. The strain in the solder joints is driven by the CTE difference between the chip and the substrate and the temperature range that the package experiences. Several strain terms were investigated using multiple linear regression techniques like those discussed at the beginning of this chapter; it was found that the incorporation of the glass transition temperature in addition to the CTE and temperature range resulted in the best input term for the predictive failure model. There are a multitude of low cycle strain based fatigue equations, based on the Coffin-Manson equation, that have been published. Many of these equations need to be used in conjunction with finite element models because they require a value for strain [inelastic

strain range, accumulated inelastic strain, creep strain range, etc.]. Although finite element modeling is widely used as a method for assessing reliability performance there is a large learning curve associated with FE modeling, hence the reason why a ‘strain term’ was incorporated into this model. This model was developed to show how regression techniques could be used to develop a predictive failure model. The next step in the modeling effort was to calculate the total inelastic strain analytically. This analytical strain was then combined with experimental results via regression analysis to generate the final predictive failure models presented in Section 5.2.5.

5.2 Analytical Model Development

In this chapter, a physics based model for the prediction of mean time to failure for a flip chip on board component was developed. The modeling effort begins with the calculation of creep and time-independent plastic strain via an analytical model. There are several assumptions associated with the analytical model: there is a perfect bond between the underfill and the silicon die (no delamination), all materials excluding solder undergo only linear elastic deformation, the radius of curvature of the laminate assembly is constant. The assumption of no delamination is important because once the underfill delaminates from the silicon die the acceleration factor for fatigue increases because the solder is no longer coupled to the underfill and the die, this results in a higher stress state at the top of the solder bump this higher stress site often corresponds to the failure site components where delamination is present. Once the creep strain and time-independent plastic strain have been calculated, the number of cycles to failure is calculated using strain based fatigue equations. The number of cycles to failure due to the plastic strain is obtained using the an analytical model along with constants developed by Soloman [Soloman, 1986]. The number of cycles to failure attributed to creep strain are calculated via a fatigue equation published by Knecht and Fox [Knecht *et al.*, 1991]. The total number of cycles to failure are calculated using Miner's Rule which combines the effects of both creep and plastic strain.

The purpose of this model is to give the designer a quick method of assessing the fatigue performance of flip chip bumps in a flip chip on organic board assembly. Recall, that fatigue of solder joints in electronic assemblies is believed to play a role in 90% of

all structural and electrical failures [Tummala 2001]. The output from the strain based fatigue calculations and the analytical model will be combined with the experimental results, using regression techniques, in Section 5.2.5. The final predictive model will incorporate not only the effects of geometry and material properties on the final fatigue performance, but will also incorporate the effects of various process induced defects and design decisions.

5.2.1 Analytical Model Introduction

Analytical, or mathematical, models are often based on a strength of materials analysis for a given package geometry. A structural analysis enables the designer to determine the induced stresses and displacements in critical design features; the feature of interest studied in this thesis is a flip chip solder joint. The purpose of these simple and easy to use models is to allow a designer to make some intelligent decisions in the design phase of a project where material selection and appropriate dimensions of structural members can be compared from the standpoint of stresses/strains and fatigue performance. When developing these analytical models there are often requirements for numerical calculations; for example, the use of the trapezoidal rule is necessary to solve the eigenvalue problem in the plastic strain calculation in the next section. Analytical tools which offer easy to use relationships are advantageous because of the clarity of the obtained information. These analytical relationships provide a clear indication of the roles of various factors affecting the given failure mechanism. This is often not the case for finite element modeling, where the input parameters are put into the system without visibility into the actual calculations that are being performed by the finite element

software. There have been numerous die-substrate analytical models developed; many of these are summarized in Table 5-4.

Table 5-4 Various Analytical Models that Have been Used in Solder Joint Fatigue Predictions

Name of the Article	Author, year
Die attachment design and Its Influence on the Thermally Induced Stresses in the Die and Attachment	Suhir, 1987
Analysis of Bi-Metal Thermostats	Timoshenko, 1925
Thermal Stresses in a Rectangular Plate Clamped Along the Edge	Aleck, 1949
Deformation of Multilayer Stacked Assemblies	Pan <i>et al</i> , 1990
Predicted Stresses in a Circular Substrate/Thin-Film System Subjected to the Change in Temperature	Suhir, 2000
Application of a Surrogate Layer for Lower Bending Stress in a Tri-Material Body	Suhir & Weld, 1996
Thermal Stresses in Bonded Joints	Chen, 1979
Stresses and Strains in a Plate Bonded to a Substrate: Semiconductor Devices	Zeyfang, 1971
Analytical Modeling of the Interfacial Shearing Stresses in Dual-coated Optical Fiber Specimens Subject to Tension	Suhir, 1993
A Creep-Rupture Model for Two-Phase Eutectic Solders	Wong, 1988

5.2.2 Suhir's Model for Bi-Metal Thermostats

Suhir in 1986 published an analytical model that was originally developed for the stresses in Bi-metal thermostats [Suhir, 1986]. In Suhir's model the tri-material system has two relatively thick layers bonded by a third layer which is a thin adhesive layer. This model is widely used in advanced electronic packaging because the structure is similar to that of a flip chip on board component level structure with an underfill layer

sandwiched in the center. This model, like most of Suhir's models, is a closed form solution that is useful for determining the effects of various material properties and geometries on the stresses in the various component layers. The model developed by Suhir is capable of predicting the axial stresses in the two layers that are being bonded by the adhesive, so for a flip chip on board example the silicon would be material 1 while the substrate would be material 2.

$$\sigma_1(x) = \frac{\Delta\alpha\Delta t}{\lambda h_1} \left(1 \pm \frac{3hD_1}{h_1 D} \right) \chi(x) \quad (5-16)$$

$$\sigma_2(x) = -\frac{\Delta\alpha\Delta t}{\lambda h_2} \left(1 \pm \frac{3hD_2}{h_2 D} \right) \chi(x) \quad (5-17)$$

Where:

h_1 = thickness of the Silicon die

h_2 = thickness of the substrate

$h = h_1 + h_2$

$\Delta\alpha = \alpha_2 - \alpha_1$

Δt = temperature increase

$$\chi(x) = 1 - \frac{\cosh(kx)}{\cosh(kl)} \quad (5-18)$$

$$D_1 \equiv \text{flexural rigidity of Silicon} = \frac{E_1 h_1^3}{12(1 - \nu_1^2)} \quad (5-19)$$

$$D_1 \equiv \text{flexural rigidity of the substrate} = \frac{E_2 h_2^3}{12(1 - \nu_2^2)} \quad (5-20)$$

Where:

$$D = D_1 + D_2 \quad (5-21)$$

E_1 & E_2 = the modulus of elasticity of the Silicon and substrate, respectively

ν_1 & ν_2 = Poisson's ratio for the Silicon and substrate, respectively

$$k = \pm \sqrt{\frac{\lambda}{\kappa}} \quad (5-22)$$

Where:

$$\lambda = \frac{1}{12} \left[\frac{h_1^2}{D_1} + \frac{h_2^2}{D_2} + \frac{3h^2}{D} \right] \quad (5-23)$$

$$\kappa = b(\kappa_1 + 2\kappa_a + \kappa_2) \quad (5-24)$$

$$\kappa_x = \frac{2(1 - \nu_x)}{3E_x} \frac{h_x}{b} \quad (5-25)$$

$$M_1(x) = \text{bending moment of Silicon} = -\frac{bh\Delta\alpha\Delta t}{2\lambda D} D_1 \chi(x) \quad (5-26)$$

$$M_2(x) = \text{bending moment of substrate} = -\frac{bh\Delta\alpha\Delta t}{2\lambda D} D_2 \chi(x) \quad (5-27)$$

$$\frac{1}{\rho(x)} = -\frac{h\Delta\alpha\Delta t}{2\lambda D} D_1 \chi(x) \quad (5-28)$$

Where:

$\rho(x)$ = radius of curvature (which is the same for materials 1 & 2)

This model is well suited for determining the stresses experienced in the die during a temperature excursion, so the model would be useful if die cracking was the failure mechanism of interest. However, other failure mechanisms such as solder fatigue cracking are not modeled as well by this method because there is a lack of stress information for the solder/underfill layer.

5.2.3 A Three Layer Analytical Model

Suhir's model was modified by Zhang in 2003 to allow for a more comprehensive three layer model [Zhang, 2003]. Zhang's model is a general equation which gives the plastic shear strain in the solder/underfill layer. This model allows a researcher to look at how various material and geometric changes affect the strain in the solder joint and ultimately the fatigue failure of the solder joint.

The analytical development work by Zhang yields the following expression for plastic shear strain in the solder joints of a flip chip on board assembly with perfectly bonded underfill [Zhang, 2003]:

$$\gamma_p(x) = \frac{\alpha_2^{xy}(\Delta T_2 - \Delta T_1)x + \frac{h_2}{3G_2}[\tau_2(x) - \tau_1(x)] + \frac{h_2 x}{\rho(x)}}{h_2 \left[1 + \alpha_2^z \left(\frac{\Delta T_1 + \Delta T_2}{2} \right) \right]} \quad (5-29)$$

Where:

α_2^{xy} = the in-plane CTE of the underfill-solder layer

h_2 = the thickness of the underfill layer

α_2^z = the z-direction CTE of the underfill-solder layer

ΔT_1 = the temperature change at the Silicon-underfill interface

ΔT_2 = the temperature change at the underfill-substrate interface

x = the distance from the center point of the chip outward

G_2 = Shear modulus of the solder underfill layer

$\rho(x)$ = the radius of curvature (assumed equal for materials 1,2, and 3)

$\tau_1(x)$ = the shear stress at the Silicon-underfill interface

$\tau_2(x)$ = the shear stress at the underfill-substrate interface

The shear modulus of the i^{th} layer of the tri-laminate structure is given by,

$$G_i = \frac{E_i}{2(1 + \nu_i)} \quad (5-30)$$

Where,

$i = 1$ for Silicon, 2 for the underfill/solder layer, and 3 for the substrate

The shear stresses at the interfaces are calculated by,

$$\tau_i(x) = C_i \sinh(kx) \quad (5-31)$$

Where,

$i = 1$ for the silicon/Underfill interface, 2 is for the underfill/substrate interface

The value for the constant C is found with the following equations,

$$C_1 = \frac{k\Delta T}{\delta \cosh kl} \left[\lambda_2(\alpha_3 - \alpha_1) + (\lambda_3 + \lambda_{23})(\alpha_2 - \alpha_1) - \sqrt{\lambda_{12}\lambda_{23}}(\alpha_3 - \alpha_2) \right] \quad (5-32)$$

$$C_2 = \frac{k\Delta T}{\delta \cosh kl} \left[\lambda_2(\alpha_3 - \alpha_1) + (\lambda_1 + \lambda_{12})(\alpha_3 - \alpha_2) - \sqrt{\lambda_{12}\lambda_{23}}(\alpha_2 - \alpha_1) \right] \quad (5-33)$$

Where,

$$\delta = \lambda_1\lambda_2 + \lambda_2\lambda_3 + \lambda_1\lambda_3 + \lambda_3\lambda_{12} + \lambda_2(\sqrt{\lambda_{12}} + \sqrt{\lambda_{23}})^2 \quad (5-34)$$

$\lambda \equiv$ the axial compliance of the i^{th} layer of the laminate

$$\lambda_{i,i+1} = \left(\frac{t_i + t_{i+1}}{2\sqrt{D}} \right)^2 \quad (5-35)$$

$D \equiv$ flexural rigidity of the individual component

$$D_i = \frac{E_i t_i^3}{12(1 - \nu_i^2)} \quad (5-36)$$

$t_i =$ thickness of the i^{th} layer of the laminate structure

$\alpha_i =$ is the CTE of the individual layers in the laminate structure; 1 is for the silicon, 2 is for the solder/underfill layer, and 3 is for the substrate

$\nu_i =$ is poisson's ratio for the individual layers in the laminate structure; 1 is for the silicon, 2 is for the solder/underfill layer, and 3 is for the substrate

The value for k is determined via numerical methods using the trapezoidal rule to be the following eigenvalues,

$$k = \pm \sqrt{\frac{(\kappa_{12}\kappa_{23}^0 + \kappa_{23}\kappa_{12}^0)^2 \pm \sqrt{(\kappa_{12}\kappa_{23}^0 + \kappa_{23}\kappa_{12}^0)^2 - 4(\kappa_{12}\kappa_{23})\delta}}{2(\kappa_{12}\kappa_{23})}} \quad (5-37)$$

Where,

$\kappa_i \equiv$ the interfacial compliance of the i^{th} layer of the laminate structure; 1 is for the silicon, 2 is for the solder/underfill layer, and 3 is for the substrate

$$\kappa_i = \frac{t_i}{3G_i} \quad (5-38)$$

$$\kappa_{ij} = \kappa_i + \kappa_j \quad (5-39)$$

$$\frac{1}{\rho(x)} = \frac{t\Delta\alpha\Delta T}{\lambda t_1} \left(1 - \frac{\cos(kx)}{\cosh(kl)} \right) \quad (5-40)$$

$l \equiv$ half the die or chip length

The analytical equation, 5-29, for plastic strain developed by Zhang can be used in conjunction with various strain based fatigue equations to predict the number of cycles to failure of a solder joint in a flip chip on board application. Although this is a useful metric in solder fatigue prediction, the creep of the solder joint should also be included.

5.2.4 Review of time dependant creep strain and selection of power law creep for analytical modeling effort

The creep of the solder joint can be calculated via various equations, many of these equations are derived from the exponential law that was presented by Norton in the 1920s [Norton, 1929].

$$\dot{\varepsilon} \equiv \frac{d\varepsilon}{dt} = k\sigma^n \quad (5-41)$$

Under small stresses, Norton's creep rule is considered applicable for time-dependent creep behavior, especially within the steady creep range. Yang, et al. used

Norton's rule to predict the ratcheting strain rate under cyclic stress histories with different dwell times [Yang, et. al 2003]. Yang presents a creep equation for a multi-level dwell time waveform.

$$\dot{\varepsilon}^r = \frac{2A}{T\dot{\sigma}} \int_{\sigma_c}^{\sigma_T} \sigma^n d\sigma + \frac{A}{T} \sigma_T^n t_T + \frac{A}{T} |\sigma_c|^n t_c \operatorname{sgn}(\sigma_c) + \frac{A}{T} |\sigma_m|^n (t_{m1} + t_{m2}) \operatorname{sgn}(\sigma_m) \quad (5-42)$$

Where,

A, n = are material constants for the solder

T = cyclic period, shown in Figure 5-7

σ_T = tensile peak stress

t_T = dwell time at the high temperature

σ_c = compressive peak stress

t_c = dwell time at the low temperature

σ_m = the mean cyclic stress

t_{m1}, t_{m2} = the start-up and shut-down dwell times

Equation 5-42 if for the thermal cycle shown in Figure 5-7.

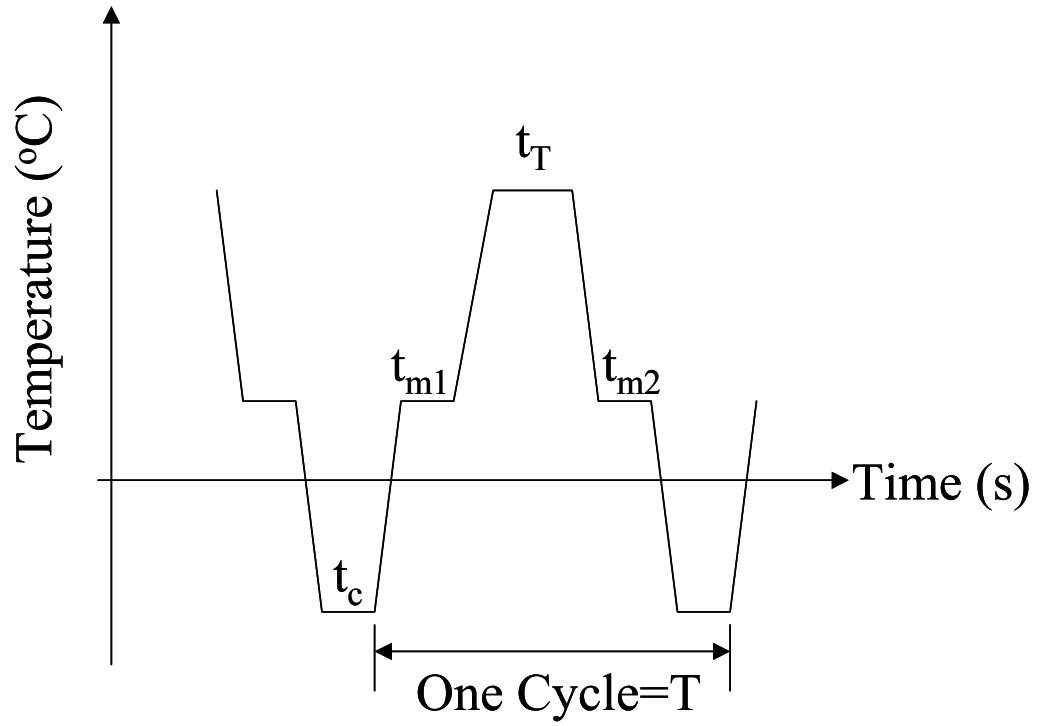


Figure 5-7 Multi-level Dwell Time Waveform

This could be generalized to a thermal cycle with 2 total dwells; one at the high temperature and one at a lower temperature; this would closely match thermal cycle and thermal shock. There are numerous other methods for assessing the creep performance of power law creep. Several researchers have broken the total strain rate into individual mechanisms of creep. For example, the climb region of creep in eutectic solder can be modeled with a traditional power law [Ju, 1994].

$$\dot{\epsilon}_c = A\sigma^n e^{-\left(\frac{Q}{R_g T}\right)} \quad (5-43)$$

Where,

A, n = are material constants for the solder

σ = current stress state

Q = activation energy for creep

R_g = Universal gas constant

T = Temperature of solder [Kelvin]

Typical creep constants have been published for eutectic 63Sn/37Pb solder [Ju, 1994] and for 62Sn/36Pb/2Ag [Pyland, 2002].

Table 5-5 Creep Constants Used for Power Law Creep of Solder Alloys (constants for Equation 5-43)

Solder Alloy	A [(Mpa) ⁻ⁿ (s) ⁻¹]	n	Q [kJ/mol]	R _g [kJ/K-mol]
63Sn/37Pb	1.84*10 ⁻⁴	5.2	50	8.314*10 ⁻³
62Sn/36Pb/2Ag	9.10*10 ⁻³	7.67	79.4	8.314*10 ⁻³

In reality there are two general creep regimes: climb and glide. The climb-controlled creep regime (which occurs at high stresses) that is presented in 5-43 is considered to be traditional “power-law” creep, and the dislocation-glide controlled regime is generally at lower stresses. The combined effects of these two creep mechanisms results in a total strain rate equation that is a double power law [Wong, 1988].

$$\dot{\epsilon}^{TOTAL} = \dot{\epsilon}^{ELASTIC} + \dot{\epsilon}^{GLIDE} + \dot{\epsilon}^{CLIMB} \quad (5-44)$$

or

$$\dot{\epsilon}^{TOTAL} = \frac{\dot{\sigma}}{E} + B_1' e^{-5413/T} \left(\frac{\sigma}{E(T)} \right)^3 + B_2' e^{-5413/T} \left(\frac{\sigma}{E(T)} \right)^7 \quad (5-45)$$

Where,

$$B'_1 = 1.7 \times 10^{12} \text{ s}^{-1}$$

$$B'_2 = 8.9 \times 10^{24} \text{ s}^{-1}$$

$E(T)$ = Elastic modulus

σ = applied stress

T = temperature in Kelvin

In addition to power law creep, there is Garofalo creep [Garofalo, 1965].

$$\dot{\gamma}_s = C_1 \frac{G}{T} \left[\sinh \left(\frac{\alpha \tau}{G} \right) \right]^n \exp \left(- \frac{Q}{kT} \right) \quad (5-46)$$

Where,

$\dot{\gamma}_s$ = shear strain rate

C_1, n, α = material constants

G = shear modulus

Q = activation energy for creep

τ = shear stress

T = temperature

k = Boltzmann's constant

With Garofola creep, traditional power law creep, double power law creep, and Wong's standard approach to creep in solder derived from Norton's creep equation there are plenty of options available to analytically model creep in solder (and there are many others available in the literature that have not been discussed in this thesis). To model the time-dependent creep behavior of solder traditional power law creep was chosen for the

analytical modeling effort. This was the method used in the finite element portion of this research to model the time-dependant behavior of solder. In summary, plastic strain was calculated with equation 5-29 and creep strain was calculated with equation 5-43.

5.2.5 Predictive Failure Model for Flip Chip on Board

In an attempt to generate a comprehensive predictive failure model for flip chip on board applications, the effects of process induced defects or design decisions must be combined with the inherent lifetime of a package. The lifetime of a “perfect” package is relatively straight forward to model with finite element software or with some simple analytical models like those in the pervious sections. However, the true lifetime of a package is also a function of things commonly not accounted for such as substrate metallization. The effects of substrate metallization on the lifetime of a component can be quantified with a correction factor, and that “correction factor” can be determined with the statistical methods discussed in Section 5.1. The correction factors can be applied to the unmodified fatigue life of the solder joint, similar to the corrections factors that are assigned to the fatigue strength of metal or machine elements, to produce a modified fatigue strength that it more representative of the actual strength of the materials in their use condition, geometry, and state. Another method for assessing the imperfectness of a package is to incorporate the correction factors into the strain based fatigue calculations directly. Correction factors for the fatigue life of a component as well as a strain based fatigue equation will be presented in this section.

5.2.5.1 Correction Factors to the Theoretical Fatigue Life Approach

The concept of attaching correction factors to an unmodified variable is not new, fatigue strengths or endurance limits are modified to account for physical differences between the actual parts in use and the parts that were used to obtain the fatigue data. Types of correction factors include those for: differences in loading conditions, temperature differences, and surface finish. An example of an endurance limit with correction factors is given by Equation 5-47 (Norton, 2000).

$$S_e = C_{load} C_{size} C_{surf} C_{temp} C_{reliab} S_e' \quad (5-47)$$

The term with the prime is the unmodified endurance limit and the term without the prime is the modified endurance limit. In this case, the correction factors can either be a number or the term can be a function of a variable. For example, the load term is either 1 for bending or 0.70 for an axial load when designing steel shafts. While the temperature term is defined as,

$$\text{For } T \leq 450^\circ\text{C} : \quad C_{temp} = 1$$

$$\text{For } 450^\circ\text{C} < T \leq 550^\circ\text{C} : \quad C_{temp} = 1 - 0.0058(T - 450)$$

The problem in assessing reliability performance is similar to the above case because the fatigue life prediction as given by an analytical calculation or via a numerical approach with finite element modeling is often physically different than the actual part that is tested. Some of the factors that influence reliability performance have been detailed in the fishbone diagram below.

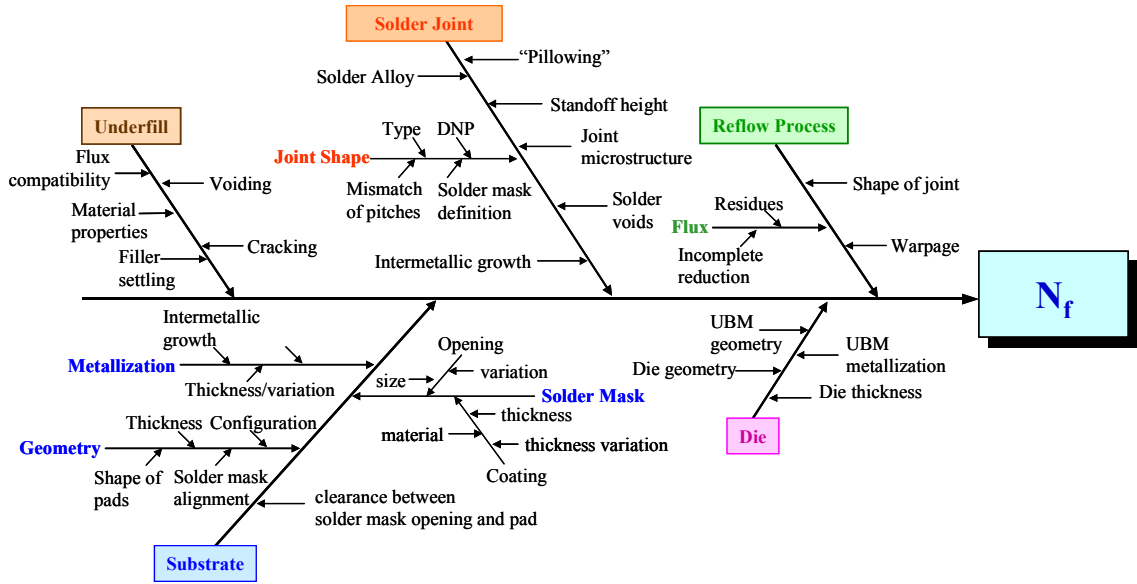


Figure 5-8 Fishbone diagram of factors that influence reliability performance of flip chip on board component level assemblies

A similar equation to 5-47 above was developed for the fatigue life of solder interconnects based on the same regression techniques described in Section 5.1. The equation takes the following form:

$$N_f = C_1 C_2 \dots C_n N_f' \quad (5-48)$$

Where, $C_1 C_2 \dots C_n$ are the modifiers to the fatigue life of the flip chip solder joint, such that the equation might take the following form:

$$N_f = C_{die\ size} \cdot C_{number\ of\ I/O} \cdot C_{solder\ alloy} \cdot C_{mask\ alignment} \dots N_f' \quad (5-49)$$

To calculate the correction factors, denoted by $C_1 C_2 \dots C_n$, a prediction of cycles to fatigue failure was needed, denoted by N_f' . The prediction of cycles to failure was conducted via analytical models, strain based fatigue equations, and Miner's Rule. The fatigue failure prediction was combined with experimental results via regression techniques to produce a corrected or 'actual' number of cycles to failure. First, the number of cycles to failure was calculated for the various experimental samples that were investigated. The total predicted cycles to fatigue failure is given by N_{total} in Table 5-6.

Table 5-6 Output of Analytical Model: Number of Cycles to Failure as a Result of Time-independent as well as Time-Dependant Strain

Die	Underfill	Test	Boards	N_{f plastic}	N_{f creep}	N_{total}
FA10 2x2	TL - Underfill D	AATS	Siemens	2737	2495	1305
	TL - Underfill C	AATS	Siemens	2797	1328	900
FA10 4x4	TL - Underfill D	AATS	Siemens	1291	2616	864
	TL - Underfill C	AATS	Siemens	1569	1407	741
PB6 2x2	TL - Underfill D	AATS	Siemens	1380	1817	784
	TL - Underfill C	AATS	Siemens	1889	1004	655
PB8 2x2	TL - Underfill D	AATS	Siemens	1635	2751	1026
	TL - Underfill C	AATS	Siemens	2189	1432	865
FA10 2x2	MC - Underfill B	AATS	Siemens AG	4424	1023	830
FA10 2x2	MC - Underfill C	AATS	Siemens AG	2281	3184	1329
FA10 2x2	MC - Underfill E	AATS	Siemens AG	4265	1084	864
FA10 2x2	MC - Underfill A	AATS	Siemens AG	4591	983	809
FA10 2x2	TL - Underfill D	LLTS	Siemens	2737	4990	1767
	TL - Underfill C	LLTS	Siemens	2797	2656	1362
FA10 4x4	TL - Underfill D	LLTS	Siemens	1291	5230	1035
	TL - Underfill C	LLTS	Siemens	1569	2812	1007
PB6 2x2	TL - Underfill D	LLTS	Siemens	1380	3634	1000
	TL - Underfill C	LLTS	Siemens	1889	2007	973
PB8 2x2	TL - Underfill D	LLTS	Siemens	1635	5502	1260
	TL - Underfill C	LLTS	Siemens	2189	2864	1241

Table 5-7 Additional No flow failure data for model

Die	Underfill	Test	Boards	N _{f plastic}	N _{f creep}	N _{total}
PB8 4x4	RT-Underfill A	AATS	4-up PB8 test vehicle (RT TV1- TV3)	1410	1310	679
	RT-Underfill A	LLTS		1410	2620	916
	RT-Underfill B	AATS		1129	2299	757
	RT-Underfill B	LLTS		1129	4598	906
	RT-Underfill C	AATS		1484	1074	623
	RT-Underfill C	LLTS		1484	2148	877
	RT-Underfill D	AATS		1121	2254	748
	RT-Underfill D	LLTS		1121	4509	897
PB8 2x2	RT-Underfill A	LLTS	Siemens (RT-TV4)	2550	2471	1255
FA10 4x4	RT-Underfill A	LLTS	3-up FA10 test vehicle (RT-TV5)	1608	2515	980
FA10 2x2	RT-Underfill A	LLTS	10-up FA10 test vehicle	3087	2364	1339

Next, the actual number of cycles to failure was needed for various experimental samples. The actual samples needed to utilize various materials, thermal cycle frequencies, substrate metallizations, processing defects, die sizes, substrate manufacturers, etc. The final experimental sample set consisted of 1160 data points which included a total of: 6 underfill materials, 2 die sizes, 9 different circuit boards, 2 substrate metallizations, 3 cyclic frequencies, and 4 test die. It was also important that the same failure mechanism was monitored for all of the modeling effort; therefore many cross-sections were completed to verify that the failure mechanism was solder joint

fatigue and another failure mechanism did not contaminate the fatigue failure data set. This was important since different failure mechanisms will accelerate failure at different rates; fortunately the test vehicles that were used throughout the experimental effort were quite simple with a basic daisy chain structure that was not useful in gathering information for mechanisms other than solder joint fatigue. The test vehicles would also identify gross solder extrusion, but this was typically visible via x-ray analysis, and the samples were not included in the data set presented in this Section.

The final model utilized simple multiple linear regression techniques to determine the correction factors for the fatigue life of solder joints. This final model assumes that the effects of cyclic frequency are included in the unmodified fatigue life term. If time-dependent plastic deformation is not included in the unmodified fatigue life term the following equation will likely overestimate the fatigue life of the solder joints.

$$N_f = C_{\text{metallization}} (\text{Pad finish}) \cdot C_{\text{joint shape}} (A_{UBM}, A_{\text{Pad}}) \cdot C_{T_g} (\text{Underfill}) \cdot N_f' \quad (5-50)$$

Where,

$$C_{\text{metallization}} = 0.038 * 1.55^M \quad (5-51)$$

The term metallization refers to the metallization of the substrate bond pads, where M is 0 for a Cu/Ni/Au finish and M is 1 for a Cu/OSP substrate bond pad finish.

$$C_{\text{joint shape}} = \left[\frac{A_{UBM}}{A_{\text{Pad}}} \right]^{-1.21} \quad (5-52)$$

A_{UBM} is the area of the under bump metallurgy and A_{pad} is the wettable pad area on the substrate.

$$C_{T_g} = T_g^{0.679} \quad (5-53)$$

Where T_g is the glass transition temperature of the underfill material that is sandwiched between the silicon die and the substrate. Recall, that N_f' is the unmodified fatigue life of the solder joints as predicted by finite element modeling or via an analytical approach.

5.2.5.2 A Strain Based Fatigue Model

A strain based fatigue model is also helpful in calculating the cycles to failure of a flip chip solder joint. The strain based models that are often employed are for low cycle fatigue and, therefore the models take the same form as the coffin-manson equation [Manson & Coffin 1965, 1954]:

$$N_f = \frac{1}{2} \left(\frac{\Delta\gamma}{2\varepsilon'_f} \right)^{1/c} \quad (5-54)$$

An analytical model can be used to calculate the strain that a solder joint experiences and various information about geometry and material specifications can be used in the predictive terms.

$$N_f = C_{\text{metallization}} (\text{Pad finish}) \cdot C_{\text{joint shape}} (A_{\text{UBM}}, A_{\text{Pad}}) \cdot C_{T_g} (\text{Underfill}) \cdot \Delta\gamma_p^{-1.29} \quad (5-55)$$

Where,

$$C_{\text{metallization}} = 0.22 * 1.70^M$$

The term metallization refers to the metallization of the substrate bond pads, where M is 0 for a Cu/Ni/Au finish and M is 1 for a Cu/OSP substrate bond pad finish.

$$C_{\text{joint shape}} = \left[\frac{A_{\text{UBM}}}{A_{\text{Pad}}} \right]^{-1.23} \quad (5-56)$$

A_{UBM} , is the area of the under bump metallurgy and A_{pad} is the wettable pad area on the substrate.

$$C_{T_g} = T_g^{0.76} \quad (5-57)$$

Where T_g is the glass transition temperature of the underfill material that is sandwiched between the silicon die and the substrate. The total plastic strain in one thermal cycle is given by $\Delta\gamma_p$.

5.2.6 Discussion of the Correction Factors

5.2.6.1 Impact of Solder Joint Shape on Reliability

Many researchers have studied the effect of flip chip solder joint shape on reliability performance. Researchers have concluded that taller solder joints with an hour glass shape have improved reliability performance over standard barrel shaped flip chip solder joints. A reliability improvement is realized because a smaller contact angle corresponds to a reduced singularity, and therefore improved fatigue performance. The contact angle of the solder on the barrel type joint is higher than that of the other types of joints and the increased contact angle corresponds to an increase in the singularity. Therefore the barrel type solder joint is the least desirable, in terms of reliability performance, out of the three types of joints presented in Figure 5-9 [Liu *et al*, 2001].

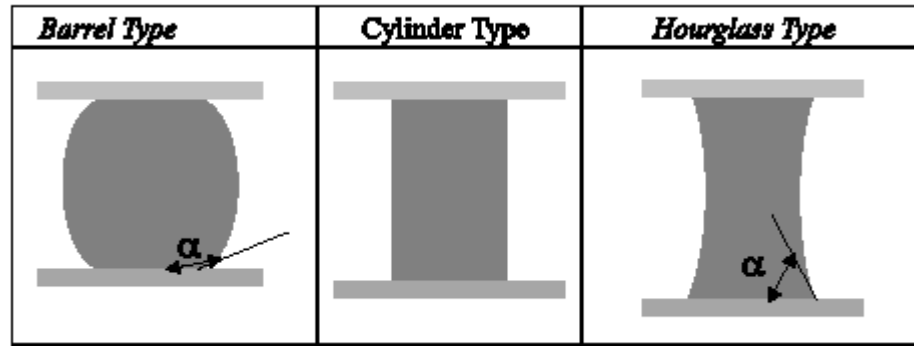


Figure 5-9 Three typical solder joint shapes (Barrel, Cylinder, and Hourglass) with contact angle differences [Liu *et al*, 2001]

All experimental samples used to generate the final reliability models presented in this thesis had barrel type solder joints. Therefore, the presented models would give a lower bound estimate of the fatigue performance of flip chip solder joints that had non-barrel type solder joints. The standoff height of the solder joint is included in the analytical model and therefore the effects height on barrel type solder joints would be predicted accurately by the presented models. Chiang *et al* have studied the effects of standoff height on barrel shaped solder joints in PBGA (plastic ball grid array) and SuperBGA assemblies [Chiang *et al*, 2000]. Solder balls A and B correspond to a solder joint on a PBGA assembly that has been reflowed twice to increase the overall standoff height, from 0.543mm in Ball A to 0.592mm in Ball B, and theoretically increase the reliability performance by increasing the compliance of the solder joint. Solder Balls C and D correspond to a solder ball on a SuperBGA assembly, where Ball D has a higher standoff than Ball C, 0.6724 mm and 0.543mm respectively.

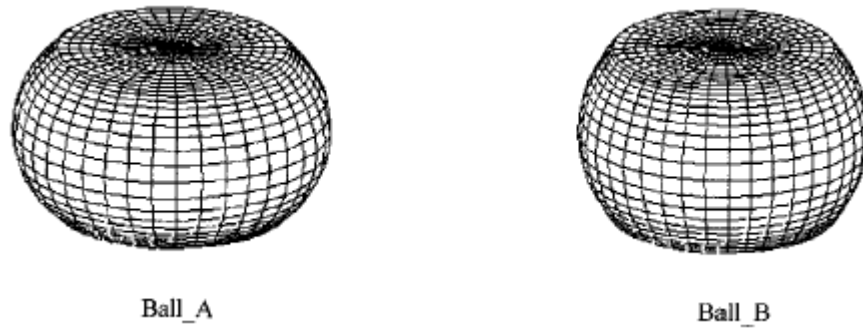


Figure 5-10 First and second reflow geometry of a PBGA solder joint; standoff for Ball A is 0.543mm and standoff for Ball B is 0.592mm [Chiang *et al.*, 2000]

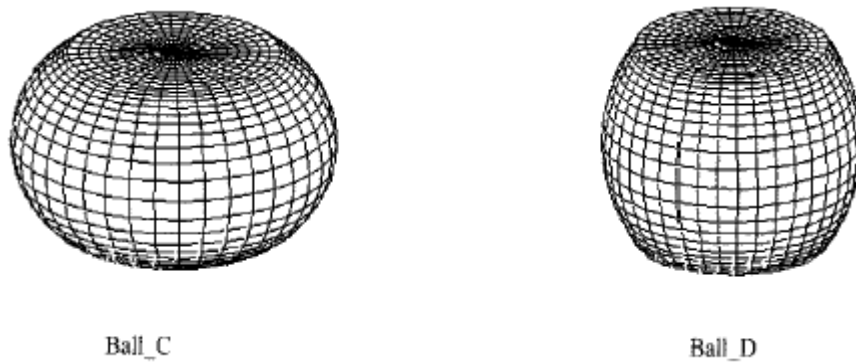


Figure 5-11 First and second reflow geometry of a SuperBGA solder joint; standoff for Ball C is 0.543mm and standoff for Ball D is 0.6724mm [Chiang *et al.*, 2000]

The increased height of the solder joint resulted in a decrease in the equivalent plastic strain which is the driving factor for low cycle strain based fatigue. The increase in solder joint height increased the predicted number of cycles to failure to increase for Ball A to 445 for Ball B.

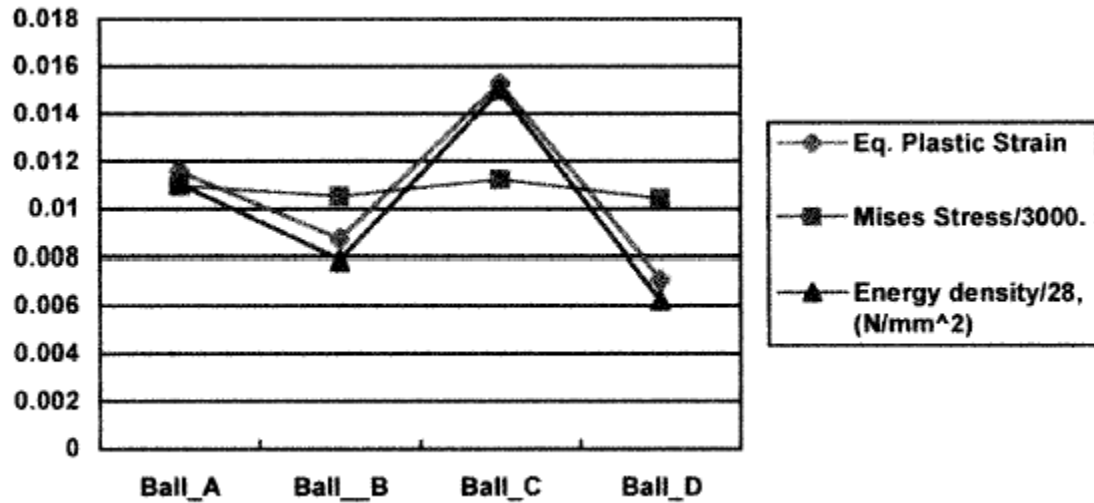


Figure 5-12 von Mises stresses and equivalent plastic strains corresponding to Balls A,B,C, and D [Chiang *et al.*, 2000]

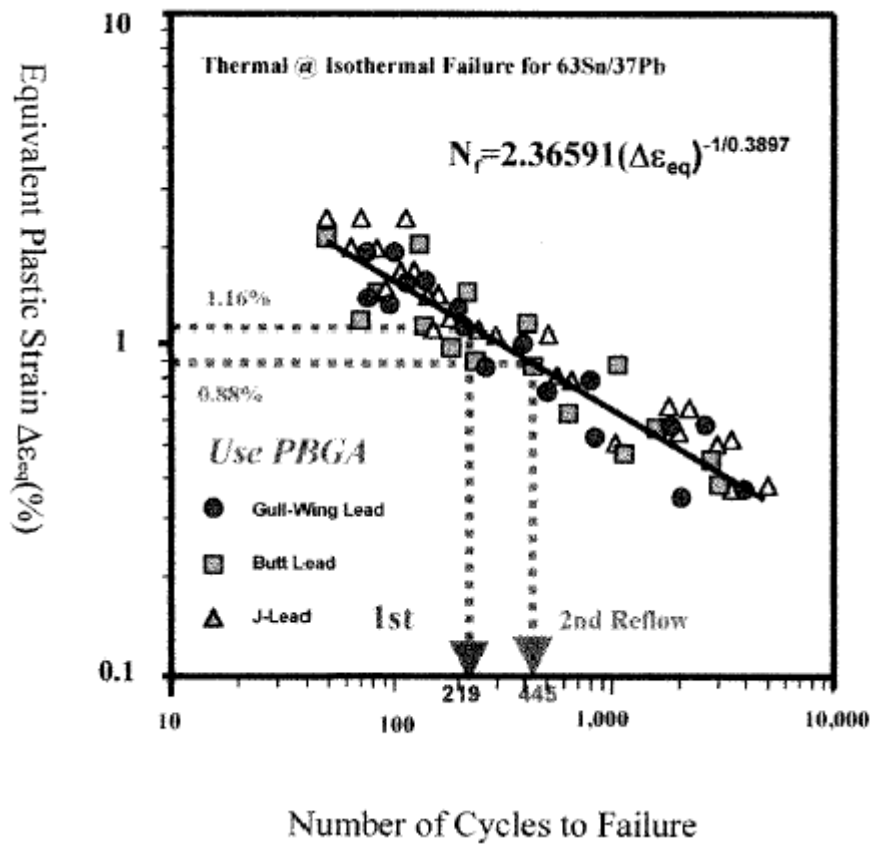


Figure 5-13 Coffin Manson Failure Model [Pao *et al.*, 1996]

Based on the Coffin-Manson failure model, low cycle strain based fatigue, prediction method an increase in reliability performance of 103% is expected with the increase in standoff height from Ball A to Ball B. An increase of 33% was predicted with the strain energy density approach for the same standoff height increase. The analytical model for plastic strain developed by Zhang along with Solomon's model predicts only a 5.65% increase in life for a flip chip on board example with a comparable increase in flip chip standoff height from 93.5 microns to 101.93 microns; this is the same 9% increase in standoff that Chiang *et al.* used for the PBGA. Chiang *et al.* realized a greater enhancement in reliability performance for the PBGA assembly with the increased standoff because the BGA bumps were not supported by underfill and the solder joint carried all the stress and strain as a result of the CTE mismatch between the PBGA and the next level of interconnection. The flip chip example shows only a small improvement in reliability performance, as would be expected for an assembly that used underfill to distribute the stresses under the die and mechanically couple the die to the substrate with underfill. Therefore, it is expected that the developed model will underpredict the effects of standoff height changes on reliability performance of bumped assemblies that do not use an underfill layer.

Substrate pads that are solder mask defined are subject to poor mask alignment or poor definition of mask openings, causing the wettable pad area to be altered. The figure below shows a mask defined substrate pad (left) and a non-solder mask defined pad (right). The SMD pad is very small in comparison to the UBM area and the NSMD pad is almost the same as the UBM diameter on the top of the flip chip solder bump.

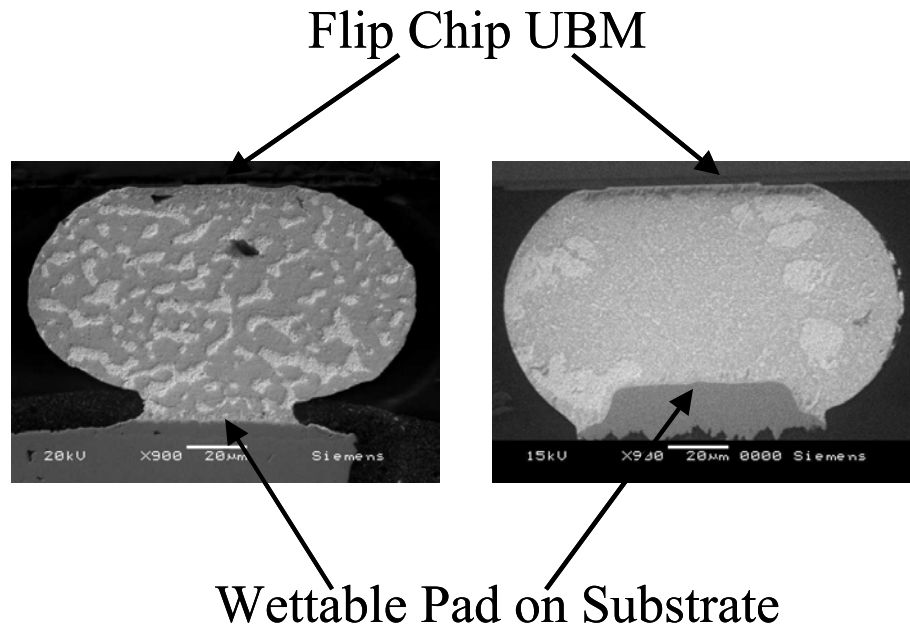


Figure 5-14 Solder Mask Defined (SMD) and non-solder mask defined (NSMD) solder joints with different solder joint shape

The solder joints for the SMD substrate pad resulted in poor reliability performance when compared to the more traditional barrel type solder joints with and equal area on the top and bottom of the joint. The effect of solder joint shape on the reliability performance of flip chip on board assemblies was studied via a 2D finite element model.

The parameter chosen to quantify the solder joint shape was the ratio of the UBM area to the wettable substrate pad area, A_{ubm} / A_{pad} . The ratio of A_{ubm} / A_{pad} was investigated using ANSYS 7.0. The ratios investigated were 0.72, 1.0 and 1.28; images of the solder joint shapes were shown in Figure 5-15.

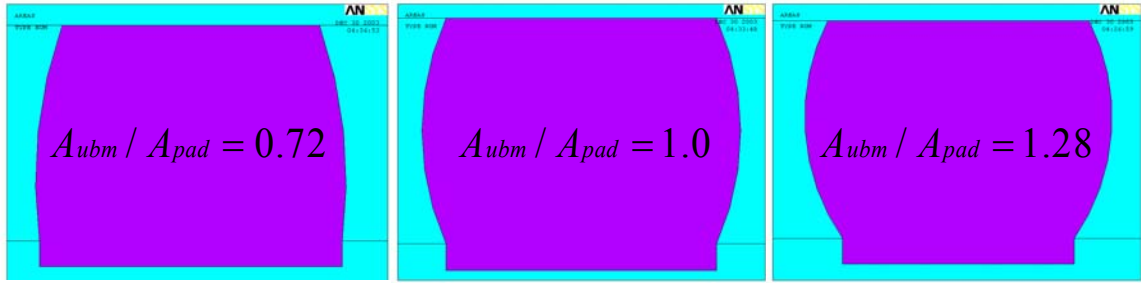


Figure 5-15 Solder Joint Shapes Investigated via FEM for Correction Factor Prediction

Term in Strain Based Fatigue Model: A_{ubm} / A_{pad} ratios 0.72, 1.0 and 1.28 studied

The area of the substrate bond pads and the UBM were both assumed to be circular, the effects of a circular UBM bonded to a rectangular bond pad could not be accurately modeled with a 2D finite element model. The plastic and creep strain for the solder joints experiencing thermal cycles from -55°C to 125 °C with 10 minute dwells was determined using ANSYS 7.0. The number of cycles to failure due to the plastic strain was determined using Cutiongco's model [Cutiongco, 1992], and the number of cycles to failure due to the creep strain was determined using the Knecht-Fox relationship [Knecht *et al.*, 1991]. The effects of plastic and creep strain were combined using the Palmgren-Miner relation to obtain a prediction of the total number of cycles to failure [Norton, 2000]. For details on this method please refer to Section 4.2. The results of this analysis showed that a ratio of 1.0 was the most desirable, a ratio of 1.275 resulted in a reduction in cycles to failure of 6.8%, while the solder joint with the ratio of 0.72 resulted in a reduction in cycles to failure of 20%.

When a circular UBM is bonded to a square substrate bond pad it is assumed that an area ratio of a little less than one would be desirable such that the cross-sectional view

of the solder joint looks similar to the solder joint with an area ratio of one in Figure 5-15.

The analytical model can be used to determine the effect of various standoff heights of the flip chip solder bumps. Since, the analytical model does not account for the shape of the solder joint a correction factor was developed to quantify effects that shape of the solder joint has on the reliability performance. Schubert et al. classified the effects of solder mask misregistration on reliability performance as negligible [Schubert *et al.*, 2000]. However, it is obvious from the finite element study presented above as well as the experimental data detailed in Chapter 6 that the relative size of the bond pads to the UBM area is an important predictor of reliability performance for a flip chip on board assembly (even if misregistration is not a factor). Therefore, the parameter chosen to quantify effects of the solder joint shape was the area of the UBM divided by the wettable pad area of the substrate bond pads, A_{ubm} / A_{pad} .

5.2.6.2 Impact of the Underfill Glass Transition Temperature on the Reliability

Performance of the Assembly

The glass transition temperature of the underfill was an important parameter to include in the model because the effects of T_g were not incorporated into the analytical model for total inelastic strain. However, if the correction factors for fatigue were used to modify a prediction of cycles to failure for a finite element model the correction factor for the glass transition temperature could be changed to 1, since the effects of the

underfill glass transition temperature were already included as material properties for the underfill material in the finite element model.

In terms of reliability performance, a low T_g underfill was not desirable because the material properties of the underfill changed drastically as the flip chip on board assembly was transitioned from a cool temperature to the junction temperature. Recall, all samples reached 125°C during air-to-air and liquid-to-liquid testing. As the temperature of the underfill exceeded the T_g , the modulus of the underfill typically changed from 1-2 GPa to ~10-15 MPa and the coefficient of thermal expansion increased from 55-75 ppm/°C to ~200 ppm/°C. This transition was quantified in Section 4.2.1.3. Therefore, while the parts are in the hot side of the thermal cycle the underfill layer provided minimal support for the solder joints. The assumed stress free temperature was 183°C meaning that the joints were likely experiencing significant creep strain while in the hot chamber.

5.2.6.3 Impact of the Substrate Metallization on the Reliability Performance

Substrate bond pad metallization, or bond pad surface finish, affect the reliability performance flip chip solder joints. Intermetallic growth provides a ‘weak link’ in the solder joint causing the intermetallic regions to serve as crack initiation as well as propagation sites. Common intermetallics such as Ni_3Sn_4 and $AuSn_4$ are brittle and can cause a solder joint to fail prematurely. The growth of these intermetallic compounds can be difficult to model in computational finite element software packages, mainly because the growth of the intermetallics is a function of unknowns (to the programmer at least)

such as the plating bath control [Watanabe, 2001]. To quantify the effects of substrate metallization on the reliability performance of the flip chip on board assemblies the circuit boards used to generate the model were plated with both Cu/Ni/Au and Cu/OSP. This provided the necessary information such that bond bad metallization could be included as a correction factor in the final low cycle strain based fatigue equation. The metallization of the substrate bond pads was noted as 'M' in the model. The probability plot for the 10mm full area array die shows a marked shift in performance between the Cu/Ni/Au and the CU/OSP substrate metallizations (Figure 5-6). This shift in performance was experienced for both underfills and all board/die configurations. Through EDX analysis it was found that there was approximately 2.8 wt% gold detectible after assembly and thermal cycling. The Au from the Cu/Ni/Au substrate pads was evenly distributed throughout the solder bump as revealed by an element mapping. The brittle intermetallic AuSn_4 forms when the gold content in a tin/lead solder joint is above 0.33 wt% [Massalski, 1987]. It is believed that the shear strength of the solder slowly decreases with increasing gold concentration above the critical limit of 0.33 wt% [Duan, 2003]. Lastly, above 3 wt% of Au the bulk solder becomes brittle and weak as a result of the excess intermetallic AuSn_4 platelets in the solder volume [Harper, 1997]. The solder joints failed in the bulk of the solder under the intermetallic formed at the UBM side of the solder joint, but the cracks did not appear to originate in the intermetallic layer. It should be noted that the flip chips used throughout this study had an Al/Ni/Cu under bump metallurgy.

6 EXPERIMENTAL RESULTS AND DISCUSSION

6.1 Experimental Reliability Results

The Air to Air Thermal Shock (AATS) and High Temperature Storage (HTS) data for the assemblies described in Sections 4.1.1.1-4.1.1.4 as well as the AATS data for the assemblies described in Section 4.1.1.5 is presented in this section. The data that is reported in this section is largely fatigue failure data for the AATS samples and creep rupture data for the assemblies that were in high temperature storage. The JEDEC pre-conditioning data, liquid to liquid thermal shock data, and the highly accelerated stress test (HAST) data was documented by Lazarakis [Lazarakis, 2003] for the assemblies described in Sections 4.1.1.1-4.1.1.4.

6.1.1 Reliability Plots: Air to Air Thermal Cycling (AATC)

Electrical resistance measurements were recorded and C-SAM images were taken of all test vehicles prior to any accelerated life testing (specifically, test vehicles described in Sections 4.1.1.1-4.1.1.5). For the AATC testing, the test vehicles were removed from the thermal cycling chamber at 100 cycle intervals such that electrical resistance measurements could be obtained. A daisy chain resistance change of $\pm 10\%$ over the original resistance measurement was considered to be an electrical failure. CSAM images were taken at regular intervals to check for delamination between the silicon chip and the underfill layer. All electrical failures were removed from test immediately after failure and failure analysis was completed. Any underfill delamination was monitored via CSAM but was not considered to be a failure.

All electrical failure data was analyzed in Minitab™ version 13.0 statistical analysis software. All failure data was plotted with a Weibull probability plot. Although the Weibull parametric distribution is typically used for modeling failures in electronics assemblies other parametric distributions were investigated via the distribution ID plot function in Minitab™. The distribution ID plot is used to show how the failure data fits four different parametric distributions, namely: Weibull, Lognormal, Exponential, and Normal. The Anderson Darling statistic was used to determine which of the distributions most closely represented the failure distribution. The Anderson-Darling statistic is used in conjunction with maximum likelihood estimation methods to compare the fit of competing distributions. The Anderson-Darling statistic is a measure of how far the plot points fall from the fitted line in a probability plot. The statistic is a weighted squared distance from the plot points to the fitted line with larger weights in the tails of the distribution. Minitab uses an adjusted Anderson-Darling statistic, because the statistic changes when a different plot point method is used. A smaller Anderson-Darling statistic indicates that the distribution fits the data better [Minitab, 2000].

The mean time to failure was calculated for the Weibull distribution for all test vehicles that were presented in this section. The mean time to failure (MTTF) is the expectation of the time to failure T and can be written as [Hayter 1996]:

$$E(T) = \int_0^{\infty} tf(t)dt \quad (6-1)$$

The mean time to failure for the Weibull distribution is:

$$MTTF_{weibull} = E(T) = \frac{1}{\lambda} \Gamma\left(1 + \frac{1}{a}\right) \quad (6-2)$$

Where λ is the scale parameter, a is the shape parameter, and $\Gamma(x)$ is the gamma function. When a is greater than one the failure rate of the components is increasing with time, the larger the value of the shape parameter, a , the steeper the increase in the failure rate of the components.

To estimate the parameters for the fitted Weibull distributions maximum likelihood estimation was used. Maximum likelihood estimates were calculated by maximizing the likelihood function. The likelihood function described, for each set of distribution parameters, the chance that the true distribution had the parameters based on the sample. Another method of estimating the parameters would be least squares estimation; where least squares estimates would be calculated by fitting a regression line to the points in a probability plot. The line would be formed by regressing time (X) to failure (Y) or log (time to failure) on the transformed percent.

For maximum likelihood estimation the distribution parameter estimates are more precise than least squares (XY). Also, MLE allows you to perform an analysis when there are no failures. When there is only one failure and some right-censored observations, the maximum likelihood parameter estimates may exist for a Weibull distribution. Therefore, maximum likelihood estimation was the method used for all parameter estimates.

All failure data was arbitrarily censored with failure times that were either interval censored or right censored. The solder joint integrity was evaluated at 100 cycle intervals, which resulted in interval censored failure data. If a part failed at the 200 cycle readout that really meant that it failed at some point between 100 cycles and 200 cycles.

Also, a few parts were removed from test to look for cracks even though they had not failed electrically; these parts were right censored because their failure interval is not known, however the last readout value is known.

6.1.1.1 PB8 2x2 OSP with TL-Underfill C

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.1. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in Figure 6-2 show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

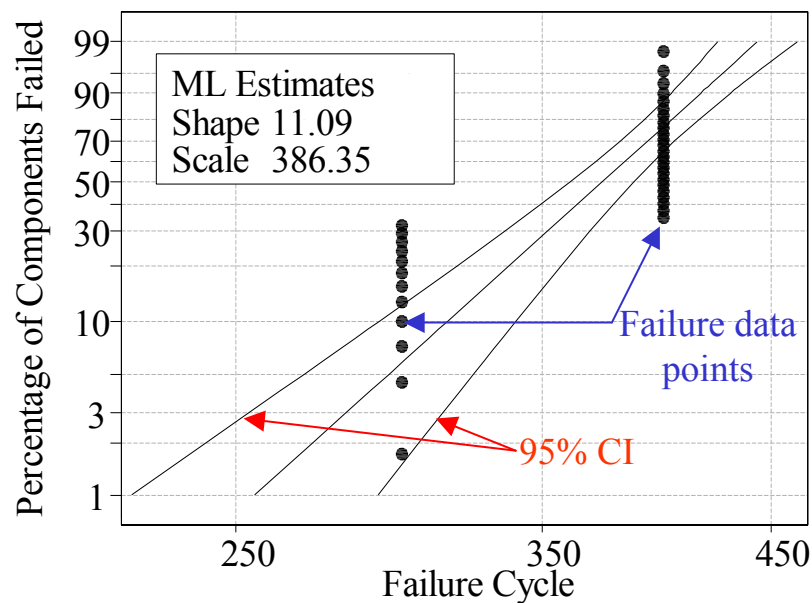


Figure 6-1 Weibull Probability Plot for PB8 2x2 OSP with TL-Underfill C

The PB8 2x2 samples did not perform very well in thermal cycle; 100% of the samples failed by 400 thermal cycles from -55 °C to 125 °C (with first failure at 300 cycles). The mean time to failure for these components was calculated to be 368 cycles;

this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above.

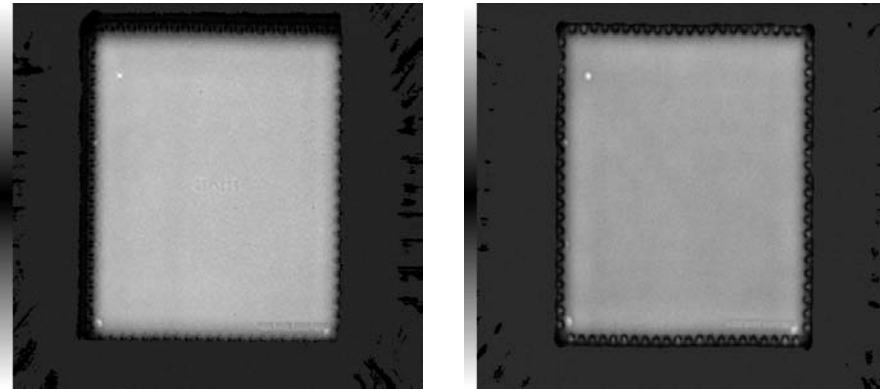


Figure 6-2 PB8 2x2 OSP TL-Underfill C, AATC CSAM results at 0 cycles and 400 cycles [no delamination]

6.1.1.2 PB8 2x2 OSP with TL-Underfill D

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.1. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in Figure 6-4 show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

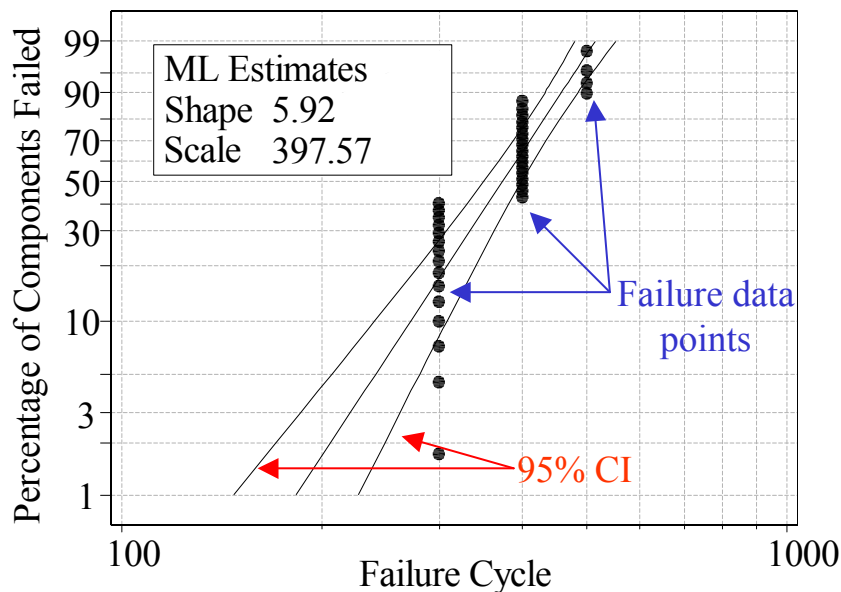


Figure 6-3 Weibull Probability Plot for PB8 2x2 OSP with TL-Underfill D

The PB8 2x2 OSP assemblies with Underfill material D performed similarly to the TL-Underfill C materials, with 100% of the parts failing by 500 cycles. First failure for these components was at 300 cycles. The mean time to failure for these components

was calculated to be 368 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above.

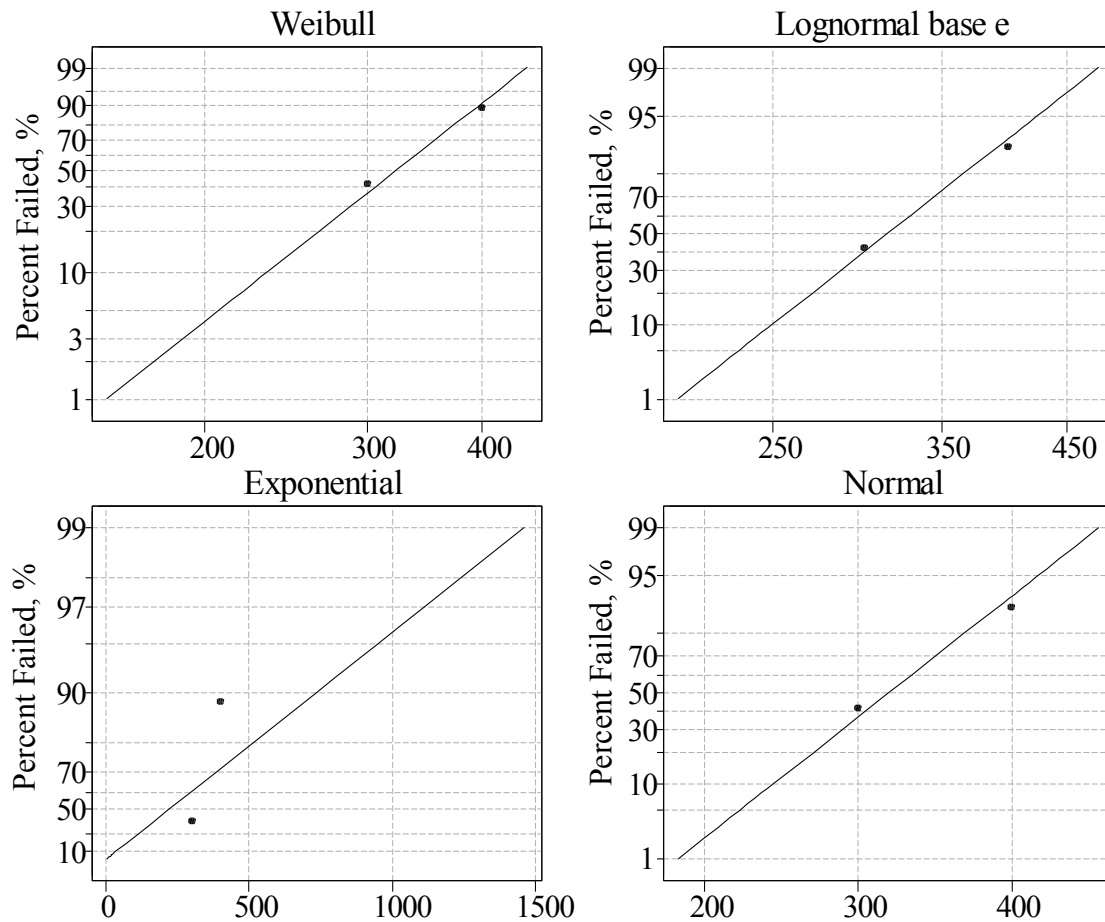


Figure 6-4 Four-Way Probability Plot PB8 2x2 OSP with TL-Underfill D, MLE, Arbitrary Censoring

Parts only failed at 3 interval ranges and this is why the distribution ID plot in Figure 6-3 shows that the Weibull, Lognormal Base e, and the Normal parametric distributions are all pretty good fits to the experimental data set (Table 6-1 for Anderson Darling Statistics). The data is plotted versus the Weibull probability plot because there

is not sufficient data to indicate that another parametric distribution would be a better fit and electrical failures typically follow a Weibull distribution.

Table 6-1 Anderson Darling Statistics for PB8 2x2 OSP with TL-Underfill D

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
PB8 2x2 OSP	Underfill D	Weibull	1.310
		Lognormal Base e	1.351
		Exponential	1.340
		Normal	1.356

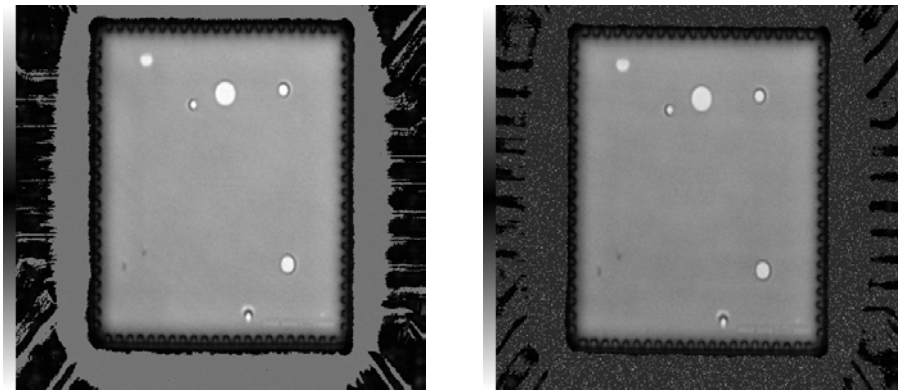


Figure 6-5 PB8 2x2 OSP TL-Underfill D, AATC CSAM results at 0 cycles and 500 cycles [no delamination]

6.1.1.3 PB8 2x2 Ni/Au with TL-Underfill C

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.1. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there

was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

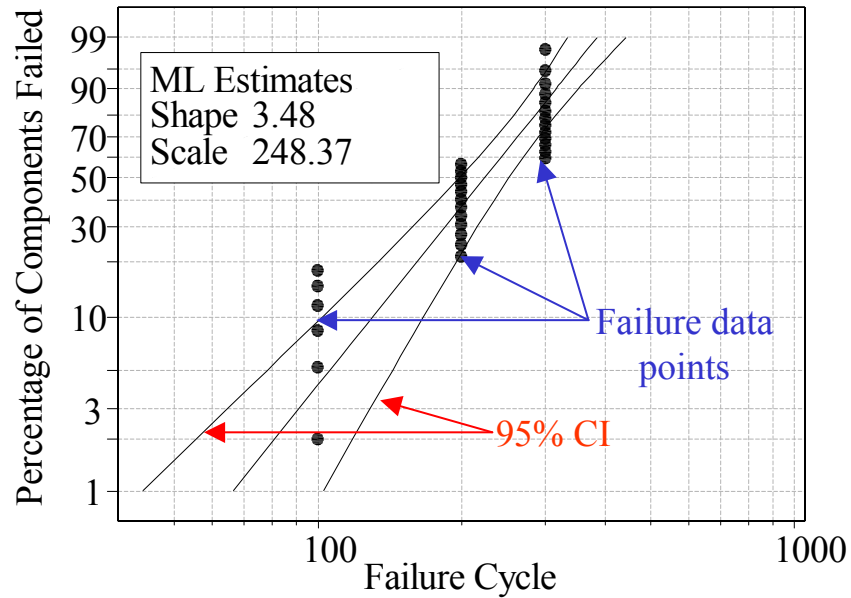


Figure 6-6 Weibull Probability Plot for PB8 2x2 Ni/Au with TL-Underfill C

The mean time to failure for these components was calculated to be 223 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure was at the 100 cycle readout and the last failure was at the 300 cycle readout.

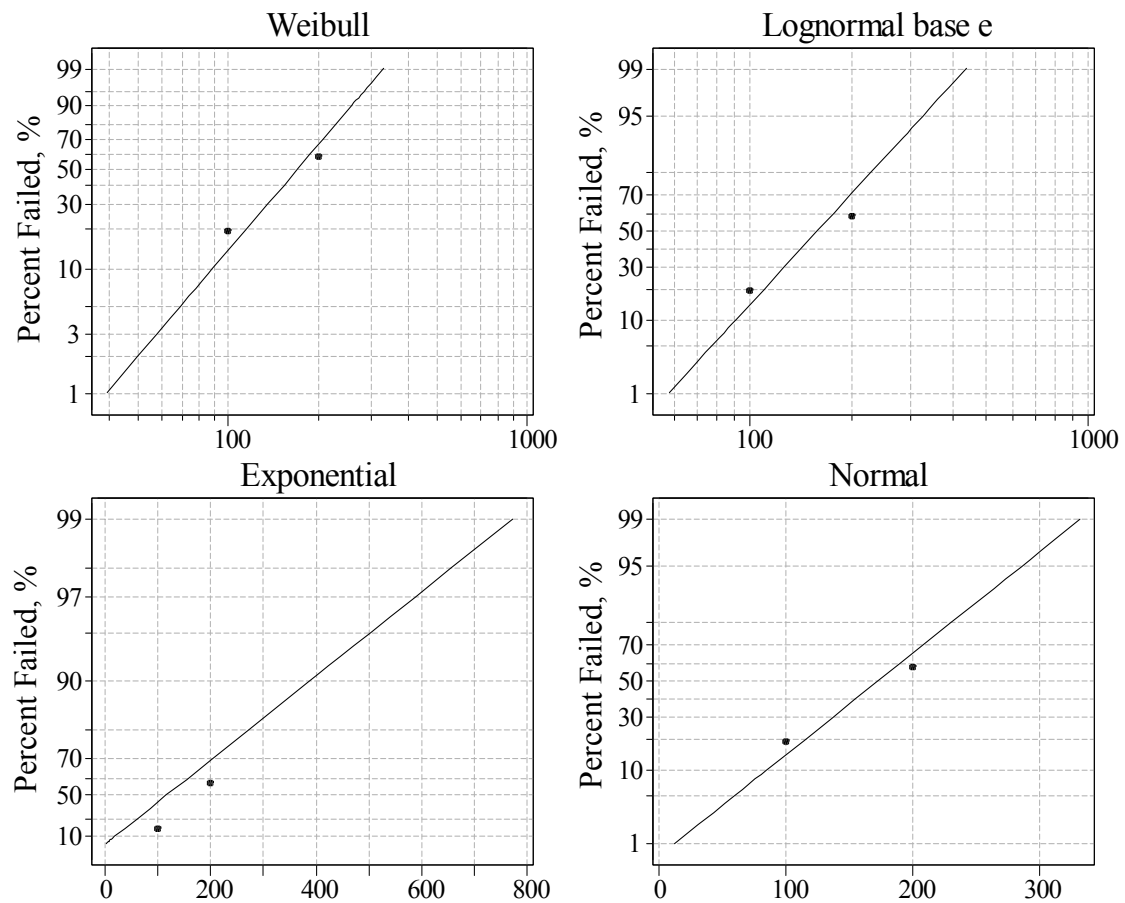


Figure 6-7 Four-Way Probability Plot PB8 2x2 Ni/Au with TL-Underfill C, MLE,
Arbitrary Censoring

Table 6-2 Anderson Darling Statistics for PB8 2x2 Ni/Au with TL-Underfill C

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
PB8 2x2 Ni/Au	Underfill C	Weibull	9.249
		Lognormal Base e	9.333
		Exponential	9.544
		Normal	9.238

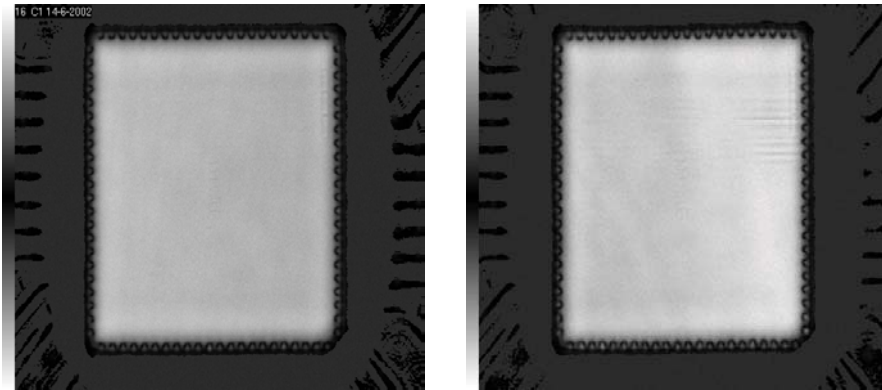


Figure 6-8 PB8 2x2 Ni/Au TL-Underfill C, AATC CSAM results at 0 cycles and 200 cycles [no delamination]

6.1.1.4 PB8 2x2 Ni/Au with TL-Underfill D

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.1. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

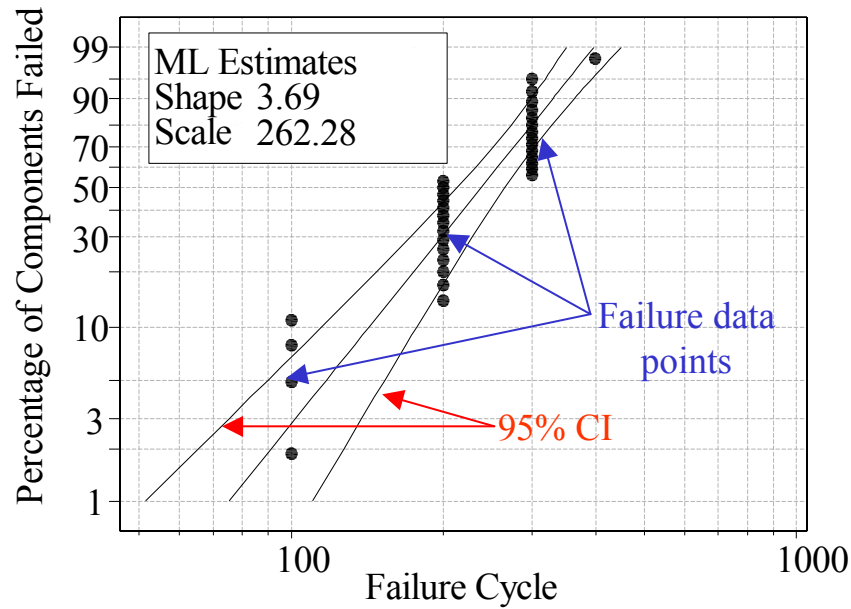


Figure 6-9 Weibull Probability Plot for PB8 2x2 Ni/Au with TL-Underfill D

The mean time to failure for these components was calculated to be 236 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for these components was at 100 cycles and the last failure was at 400 cycles. Please note that these samples performed significantly worse than the PB8 2x2 OSP samples with the same underfill, TL-Underfill D, with a MTTF of 236 cycles versus the 368 cycles for the OSP substrates. This trend in reliability performance between the Cu/Ni/Au substrates and the Cu/OSP substrates was apparent for all of the substrates that were tested in AATC; this difference in performance was also realized in some of the other accelerated life tests, such as High Temperature Storage Life. The results of HTS are discussed in the next section of this Chapter.

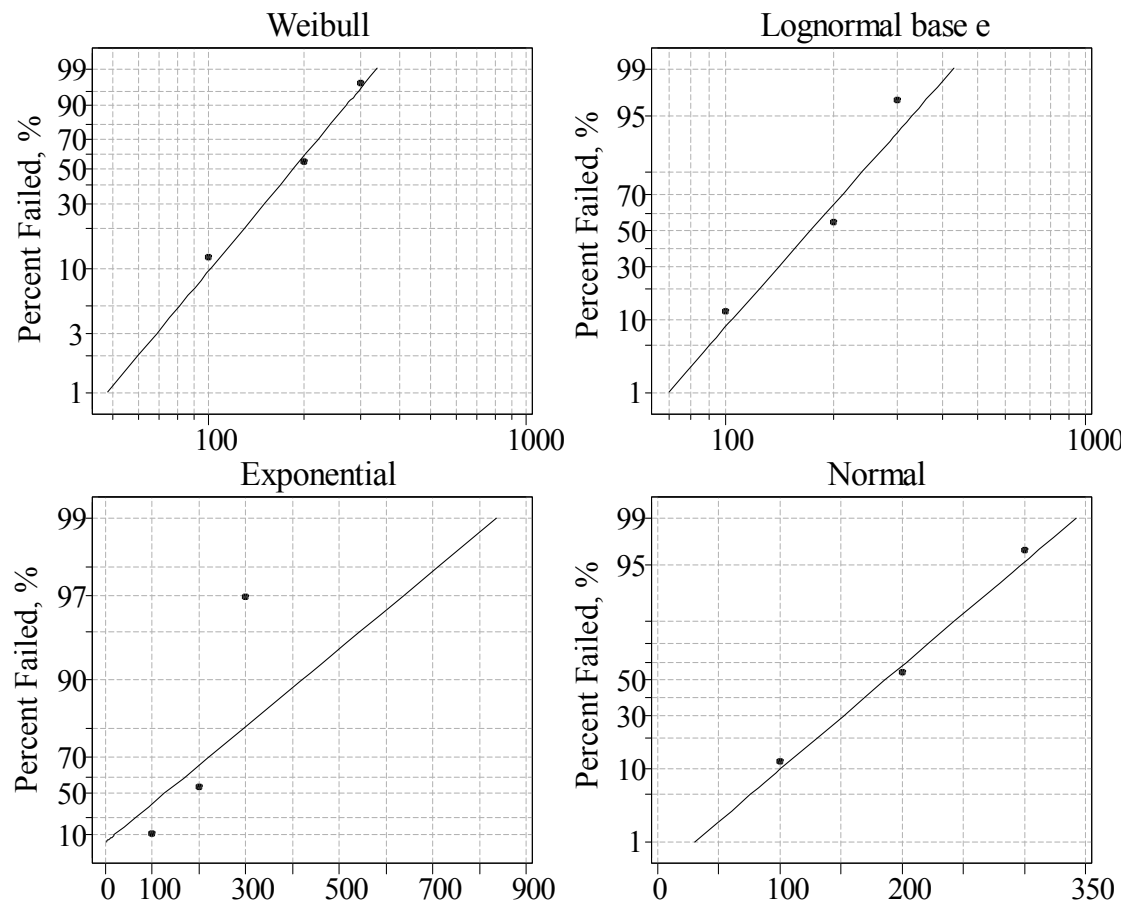


Figure 6-10 Four-Way Probability Plot PB8 2x2 Ni/Au with TL-Underfill D, MLE, Arbitrary Censoring

Table 6-3 Anderson Darling Statistics for PB8 2x2 Ni/Au with TL-Underfill D

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
PB8 2x2 Ni/Au	Underfill D	Weibull	1.212
		Lognormal Base e	1.081
		Exponential	1.129
		Normal	1.193

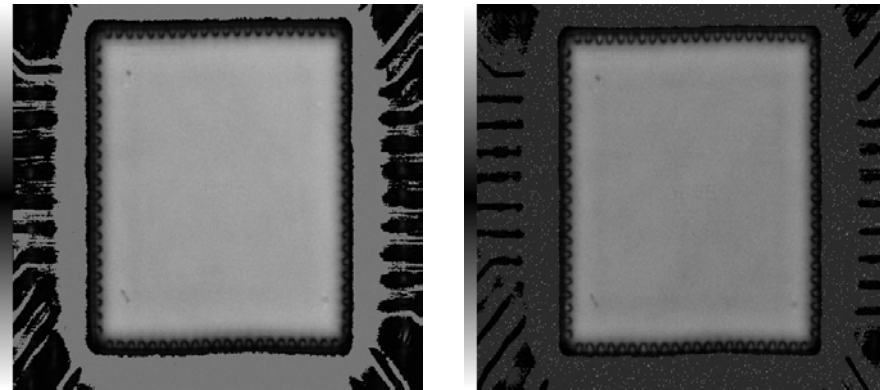


Figure 6-11 PB8 2x2 Ni/Au TL-Underfill D, AATC CSAM results at 0 cycles and 400 cycles [no delamination]

6.1.1.5 PB6 2x2 OSP with TL-Underfill C

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.2. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

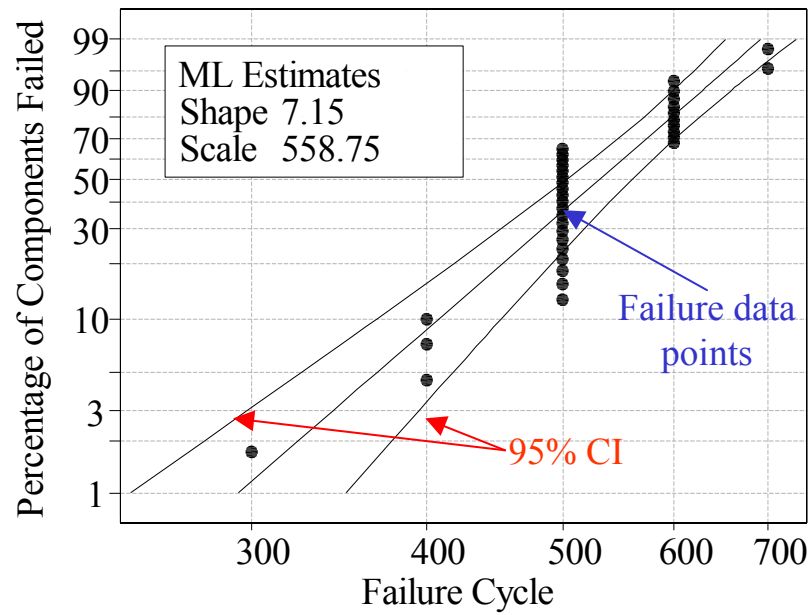


Figure 6-12 Weibull Probability Plot for PB6 2x2 OSP with TL-Underfill C

The mean time to failure for these components was calculated to be 523 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for this component was at 300 cycles and the last failure was at 700 cycles.

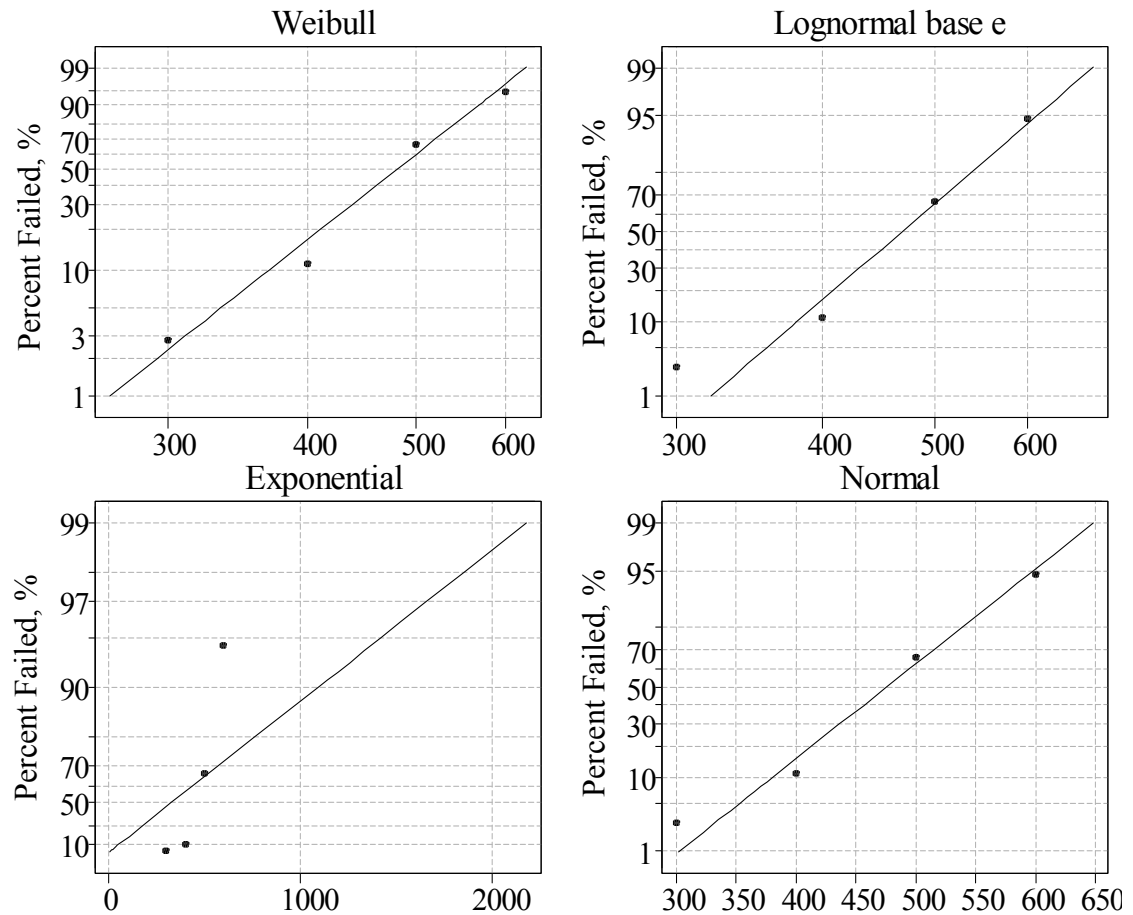


Figure 6-13 Four-Way Probability Plot PB6 2x2 OSP with TL-Underfill C, MLE, Arbitrary Censoring

Table 6-4 Anderson Darling Statistics for PB6 2x2 OSP with TL-Underfill C

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
PB6 2x2 OSP	Underfill C	Weibull	1.443
		Lognormal Base e	1.484
		Exponential	1.780
		Normal	1.469

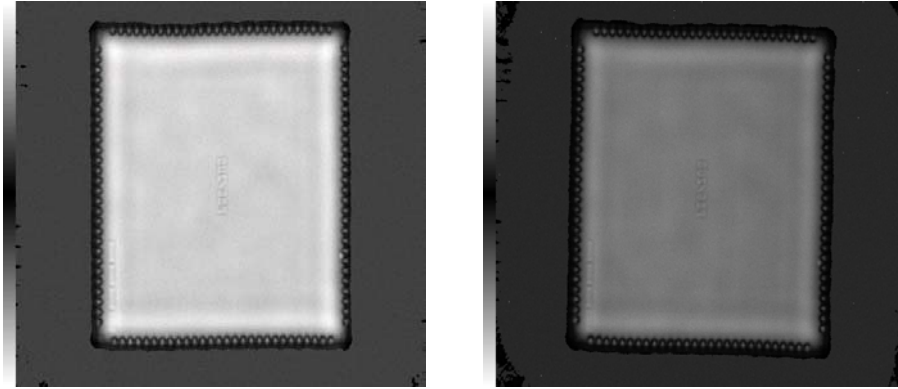


Figure 6-14 PB6 2x2 OSP with TL-Underfill C: CSAM images at 0 cycles (left) and 700 cycles (right), no delamination

6.1.1.6 PB6 2x2 OSP with TL-Underfill D

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.2. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

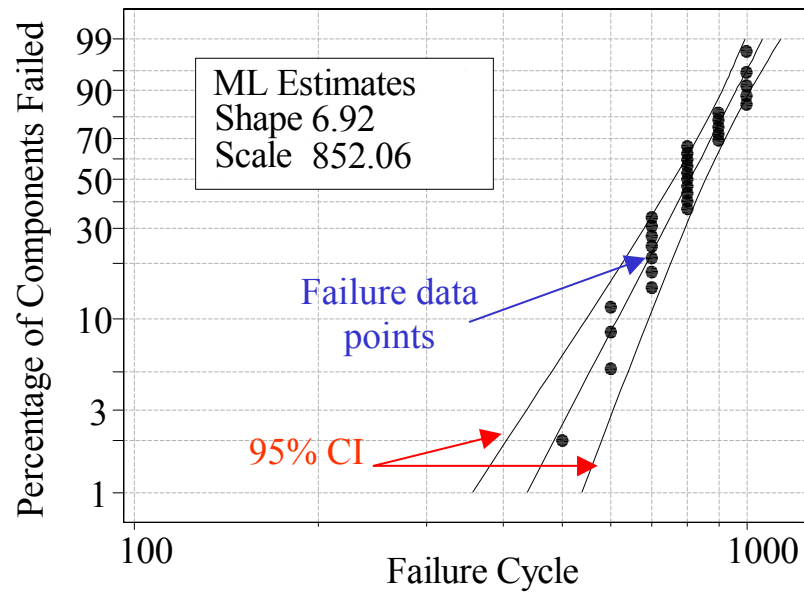


Figure 6-15 Weibull Probability Plot for PB6 2x2 OSP with TL-Underfill D

The mean time to failure for these components was calculated to be 796 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure was at 500 cycles and all components failed by 1000 cycles.

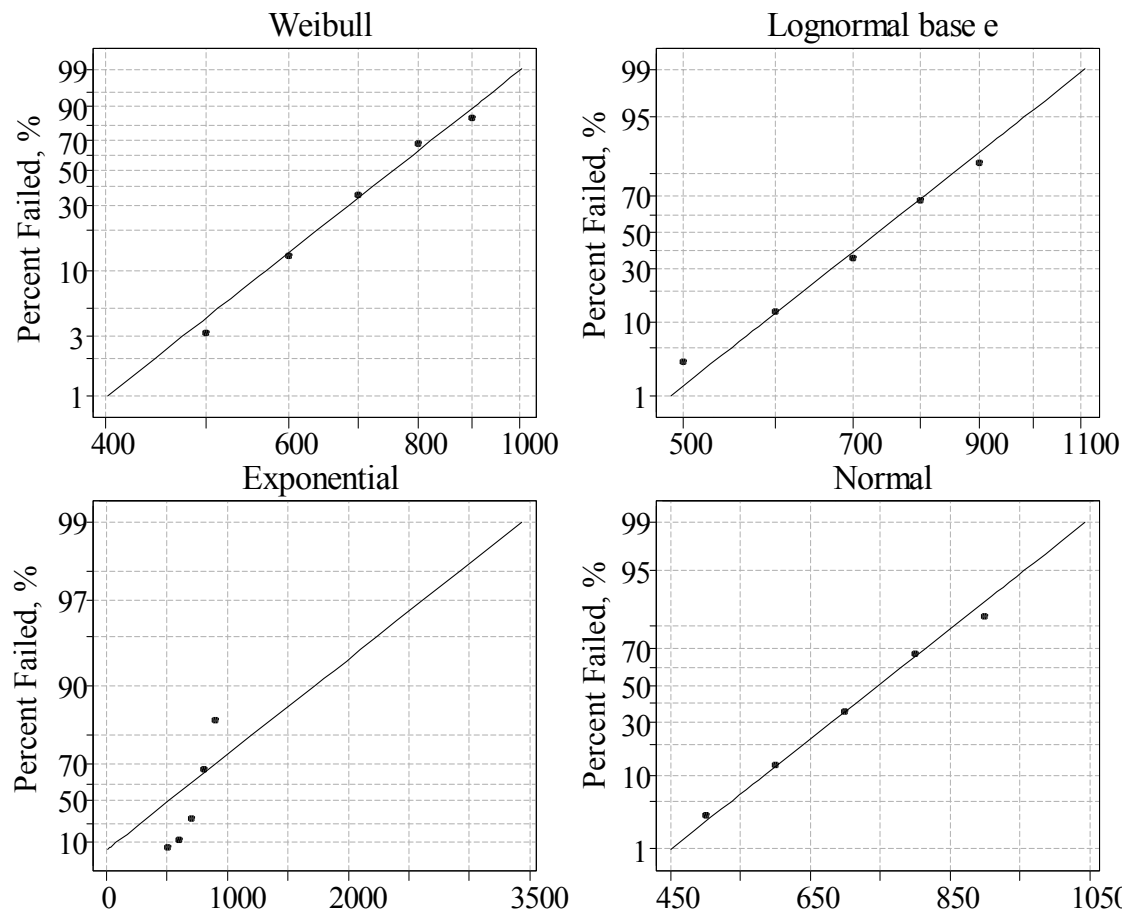


Figure 6-16 Four-Way Probability Plot PB6 2x2 OSP with TL-Underfill D, MLE, Arbitrary Censoring

Table 6-5 Anderson Darling Statistics for PB6 2x2 OSP with TL-Underfill D

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
PB6 2x2 OSP	Underfill D	Weibull	3.531
		Lognormal Base e	3.661
		Exponential	4.728
		Normal	3.595

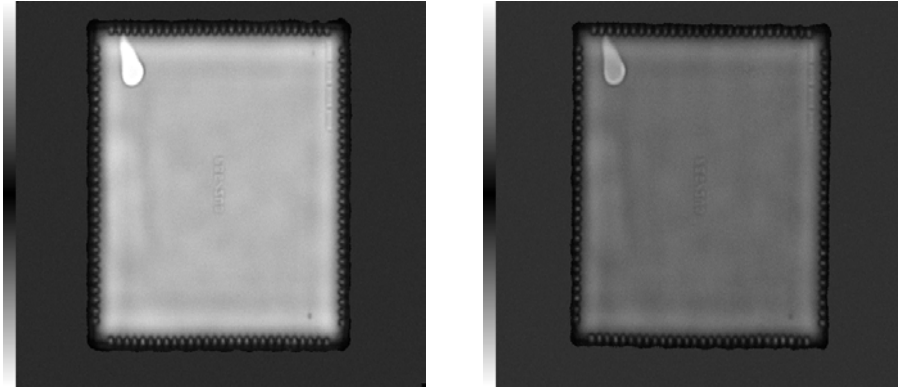


Figure 6-17 PB6 2x2 OSP with TL-Underfill D: CSAM images at 0 cycles (left) and 1000 cycles (right), no delamination

6.1.1.7 PB6 2x2 Ni/Au with TL-Underfill C

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.2. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

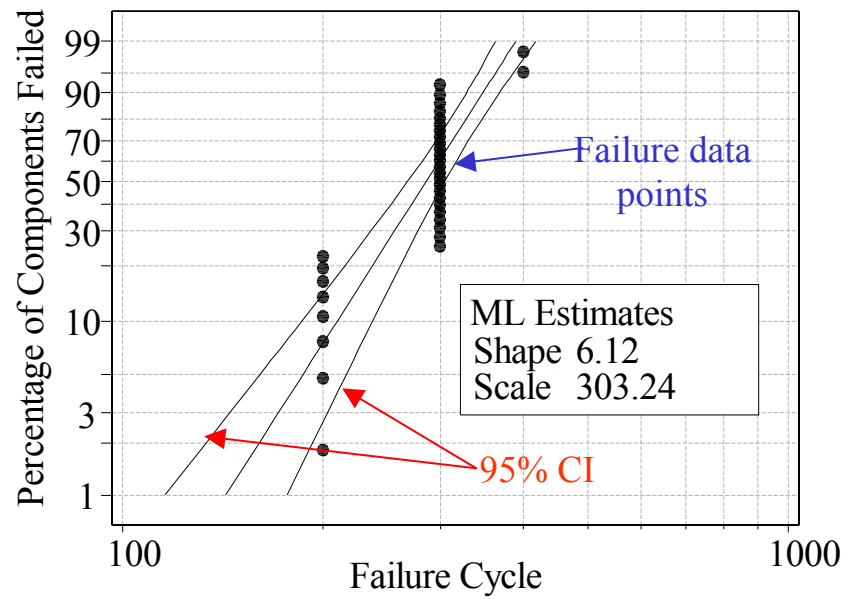


Figure 6-18 Weibull Probability Plot for PB6 2x2 Ni/Au with TL-Underfill C

The mean time to failure for these components was calculated to be 281 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for this test vehicle was at 200 cycles and the last failure was at 400 cycles.

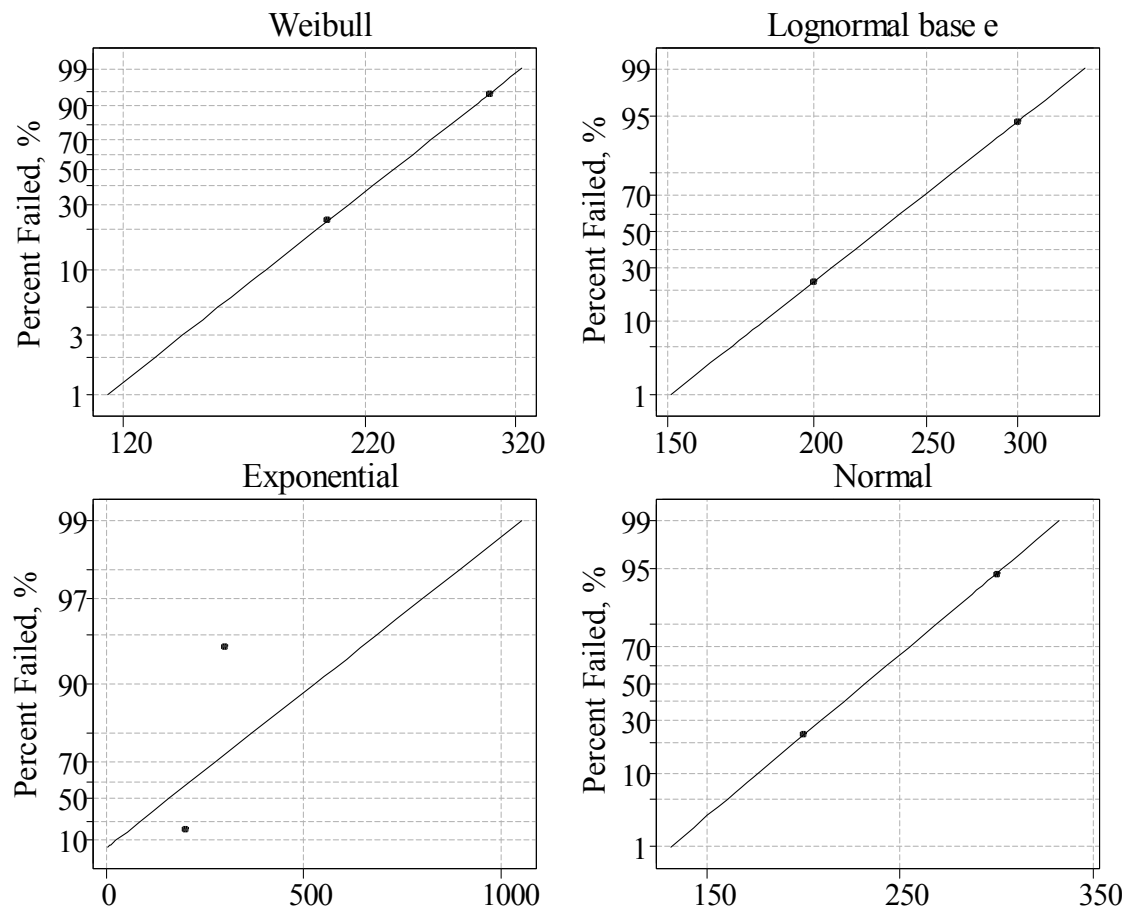


Figure 6-19 Four-Way Probability Plot PB6 2x2 Ni/Au with TL-Underfill C, MLE,
Arbitrary Censoring

Table 6-6 Anderson Darling Statistics for PB6 2x2 Ni/Au with TL-Underfill C

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
PB6 2x2 Ni/Au	Underfill C	Weibull	2.001
		Lognormal Base e	1.991
		Exponential	1.023
		Normal	1.998

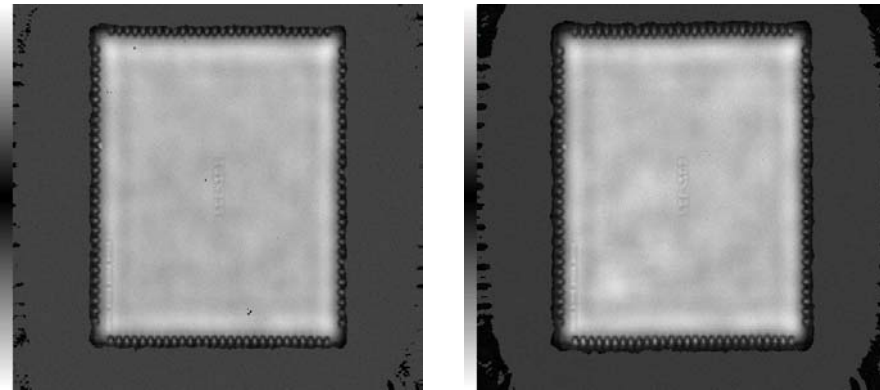


Figure 6-20 PB6 2x2 Ni/Au with TL-Underfill C: CSAM images at 0 cycles (left) and 300 cycles (right), no delamination

6.1.1.8 PB6 2x2 Ni/Au with TL-Underfill D

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.2. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

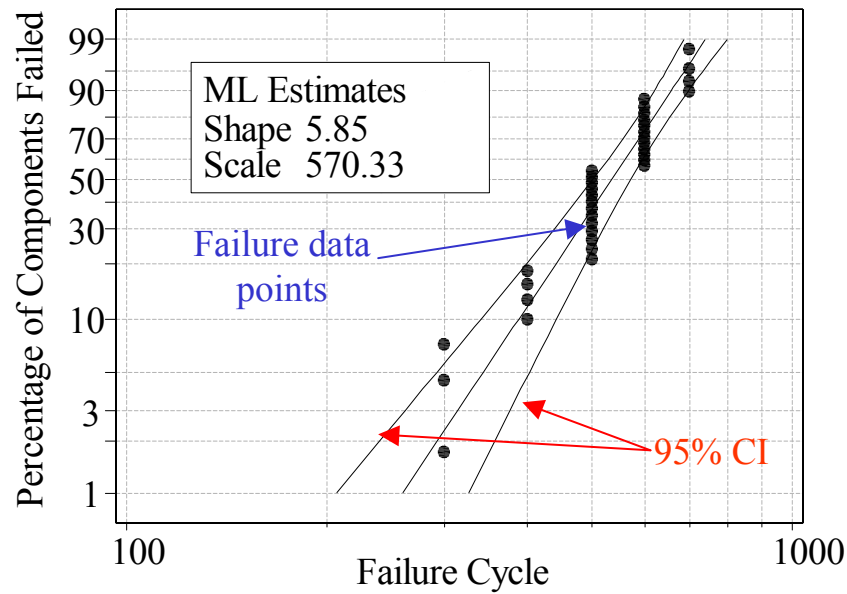


Figure 6-21 Weibull Probability Plot for PB6 2x2 Ni/Au with TL-Underfill D

The mean time to failure for these components was calculated to be 528 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure was at 300 cycles and all parts had failed by 700 cycles. Again, notice that the MTTF for the samples with the OSP substrate metallization was 796 cycles to failure and the MTTF for the Ni/Au substrate metallization samples was 528 cycles. TL-Underfill D again outperformed TL-Underfill C for this test vehicle.

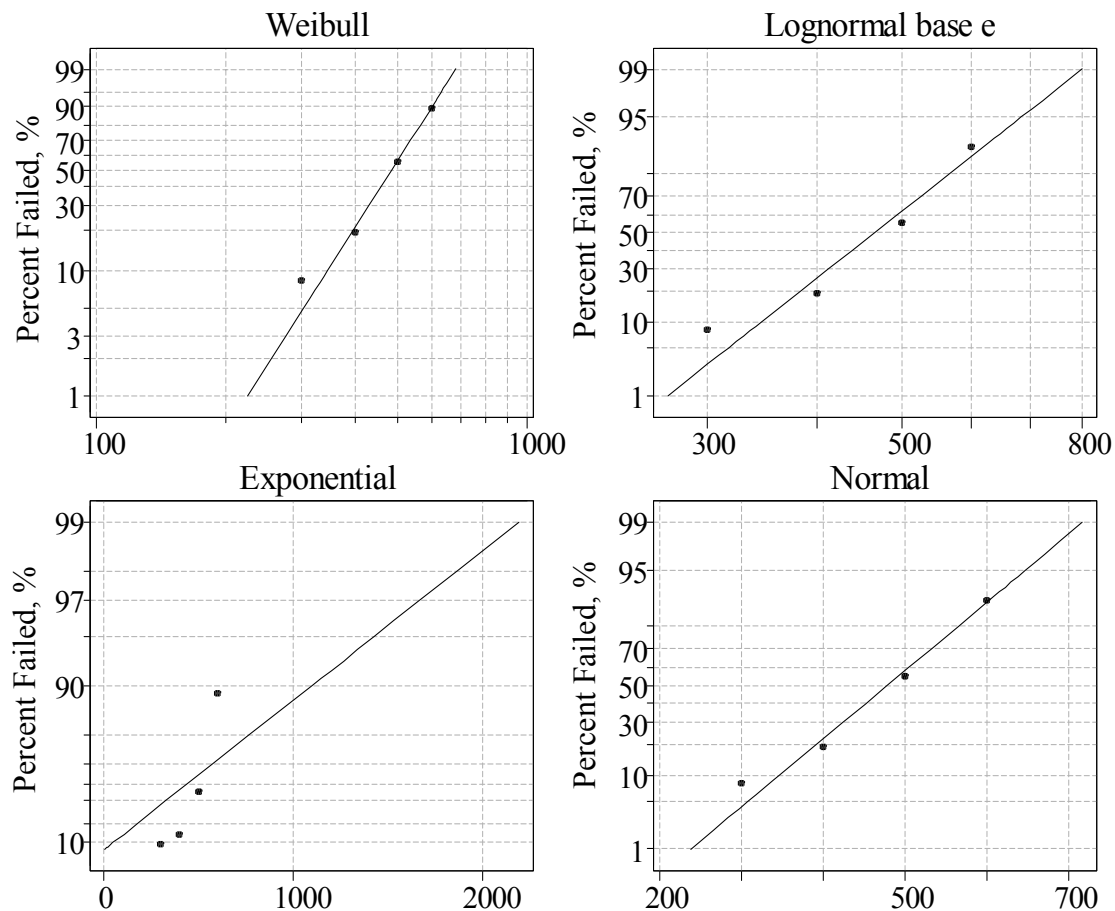


Figure 6-22 Four-Way Probability Plot PB6 2x2 Ni/Au with TL-Underfill D, MLE, Arbitrary Censoring

Table 6-7 Anderson Darling Statistics for PB6 2x2 Ni/Au with TL-Underfill D

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
PB6 2x2 Ni/Au	Underfill D	Weibull	1.846
		Lognormal Base e	1.891
		Exponential	2.440
		Normal	1.856

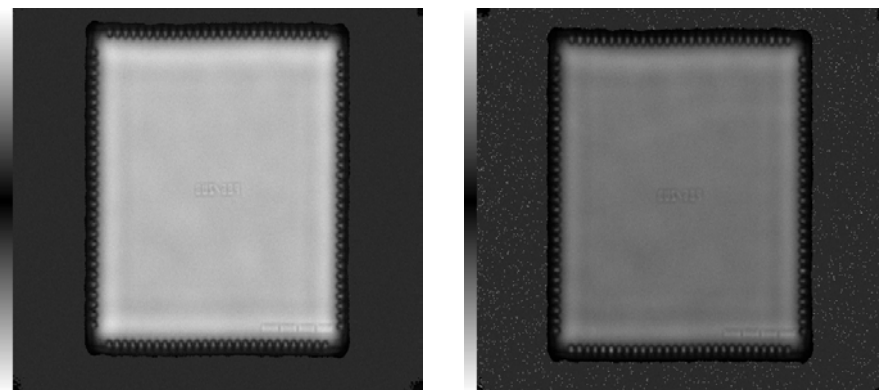


Figure 6-23 PB6 2x2 Ni/Au with TL-Underfill D: CSAM images at 0 cycles (left) and 700 cycles (right), no delamination

6.1.1.9 FA10 2x2 OSP with TL-Underfill C

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.4. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

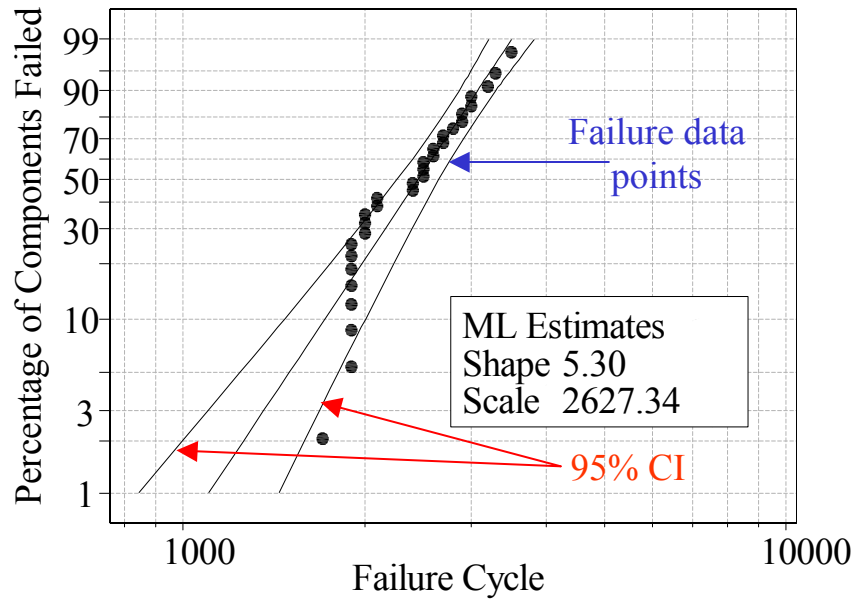


Figure 6-24 Weibull Probability Plot for FA10 2x2 OSP with TL-Underfill C

The mean time to failure for these components was calculated to be 2420 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for these components was at 1700 cycles and the last failure was at 3500 cycles. This test vehicle and material set performed the best, meaning the highest MTTF, out of all of the samples that were evaluated in air to air thermal shock.

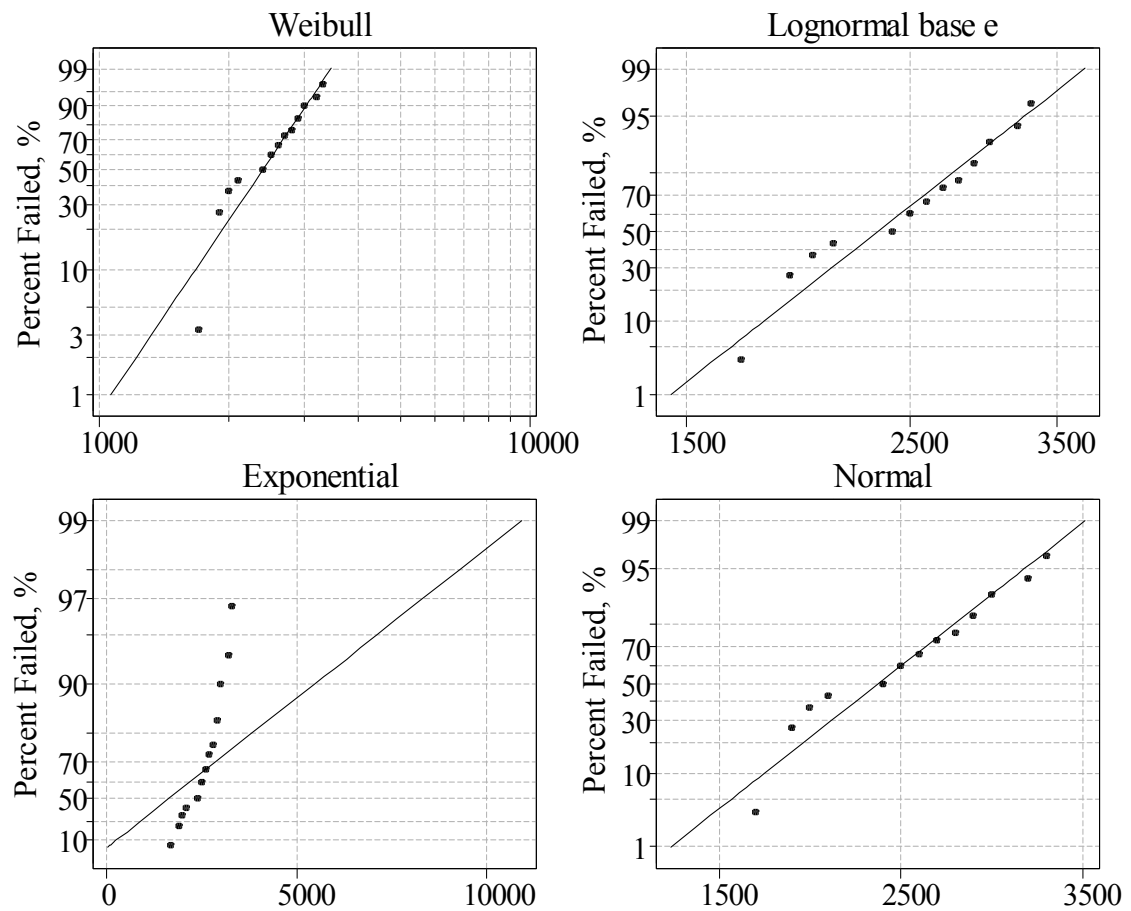


Figure 6-25 Four-Way Probability Plot FA10 2x2 OSP with TL-Underfill C, MLE,
Arbitrary Censoring

Table 6-8 Anderson Darling Statistics for FA10 2x2 OSP with TL-Underfill C

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
FA10 2x2 OSP	Underfill C	Weibull	0.690
		Lognormal Base e	0.744
		Exponential	4.116
		Normal	0.722

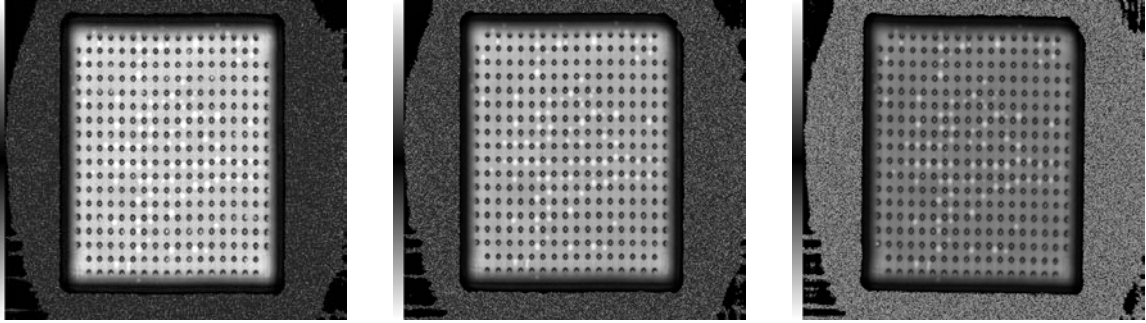


Figure 6-26 FA10 2x2 OSP with TL-Underfill C: CSAM images at 0 cycles (left), 1000 cycles, and 1800 cycles (right), no delamination

6.1.1.10 FA10 2x2 OSP with TL-Underfill D

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.4. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

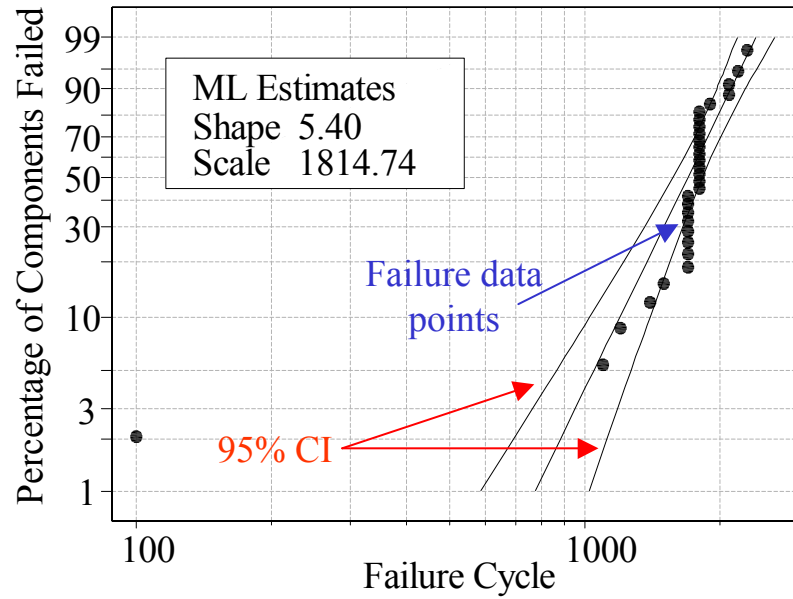


Figure 6-27 Weibull Probability Plot for FA10 2x2 OSP with TL-Underfill D

The mean time to failure for these components was calculated to be 1674 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for these components was at 1100 cycles and the last failure was at 2300 cycles. Notice that TL-Underfill C outperformed TL-Underfill D for this test vehicle, where the opposite was realized for the perimeter array test vehicles discussed in the preceding sections of this Chapter.

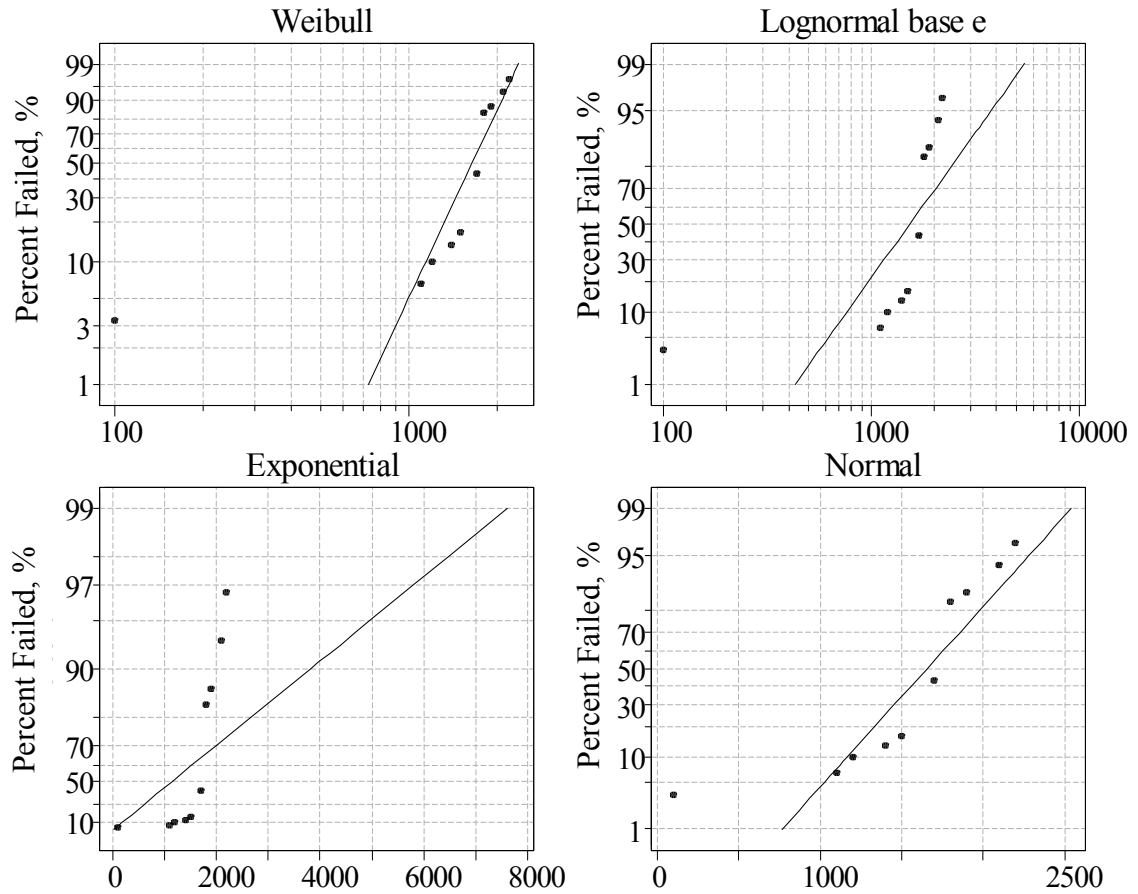


Figure 6-28 Four-Way Probability Plot FA10 2x2 OSP with TL-Underfill D, MLE,
Arbitrary Censoring

Table 6-9 Anderson Darling Statistics for FA10 2x2 OSP with TL-Underfill D

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
FA10 2x2 OSP	Underfill D	Weibull	1.594
		Lognormal Base e	2.363
		Exponential	3.368
		Normal	1.450

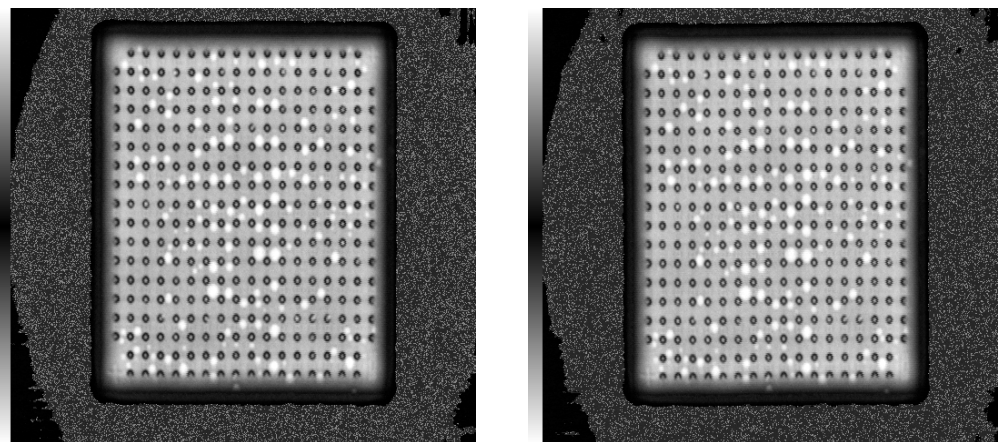


Figure 6-29 FA10 2x2 OSP with TL-Underfill D: CSAM images at 0 cycles (left), 2100 cycles (right), no delamination

6.1.1.11 FA10 2x2 Ni/Au with TL-Underfill C

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.4. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

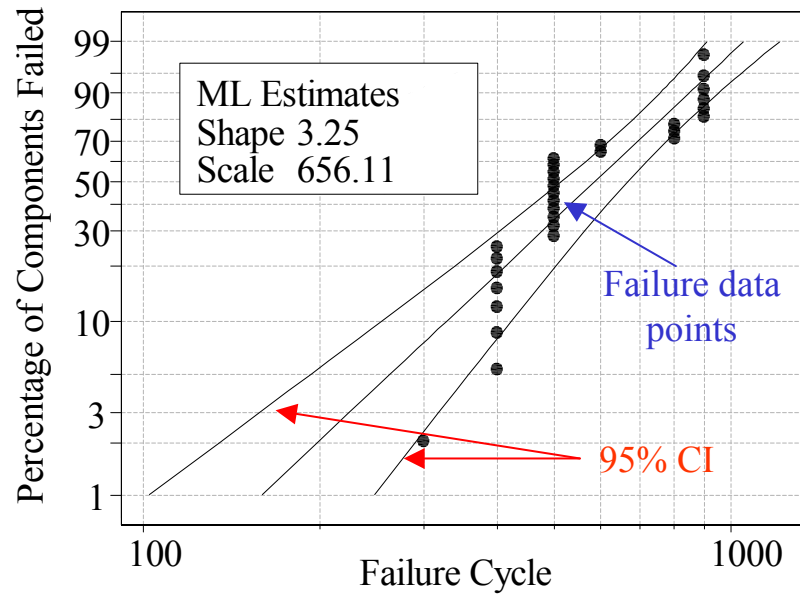


Figure 6-30 Weibull Probability Plot for FA10 2x2 Ni/Au with TL-Underfill C

The mean time to failure for these components was calculated to be 588 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for these components was at 300 cycles and the last failure was at 900 cycles. Again, notice the discrepancy in performance between the Ni/Au and OSP substrate metallization test vehicles; Ni/Au with a MTTF of 588 cycles and OSP with a MTTF of 2420 cycles.

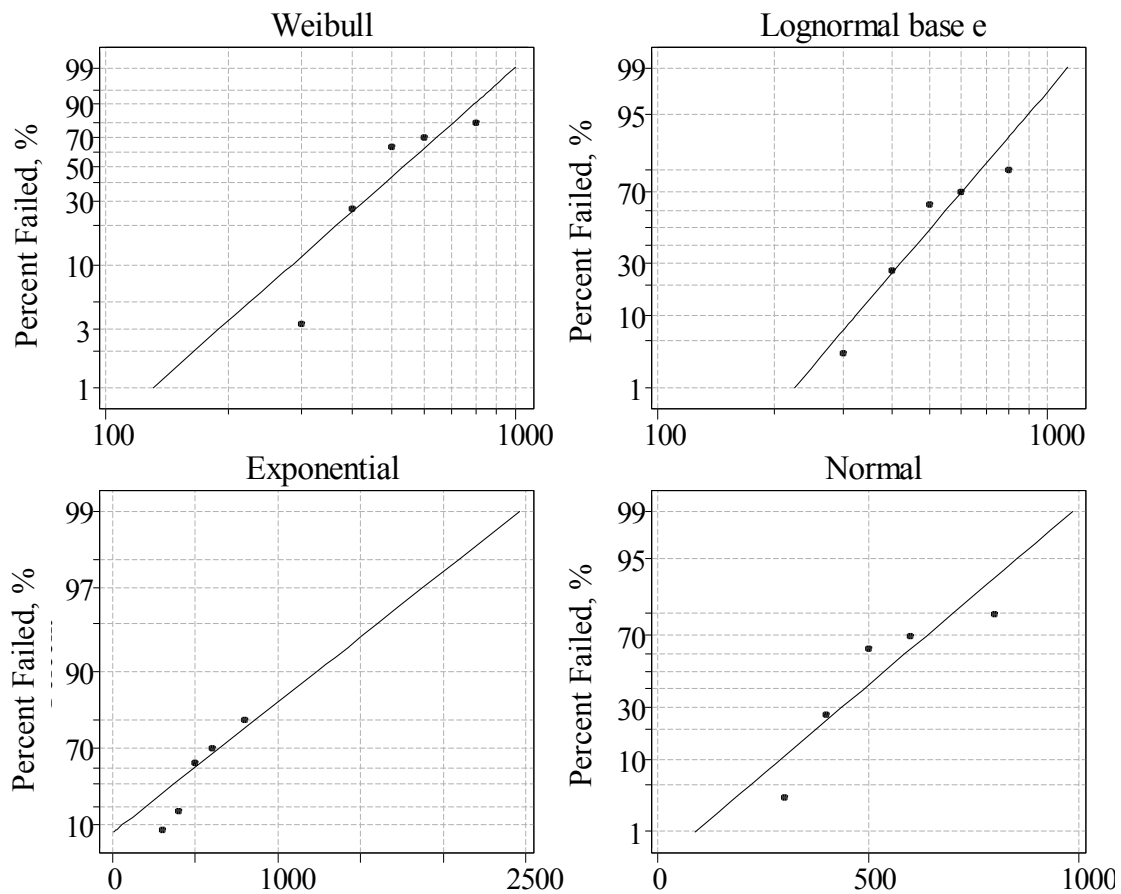


Figure 6-31 Four-Way Probability Plot FA10 2x2 Ni/Au with TL-Underfill C, MLE, Arbitrary Censoring

Table 6-10 Anderson Darling Statistics for FA10 2x2 Ni/Au with TL-Underfill C

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
FA10 2x2 Ni/Au	Underfill C	Weibull	5.251
		Lognormal Base e	5.251
		Exponential	6.118
		Normal	5.255

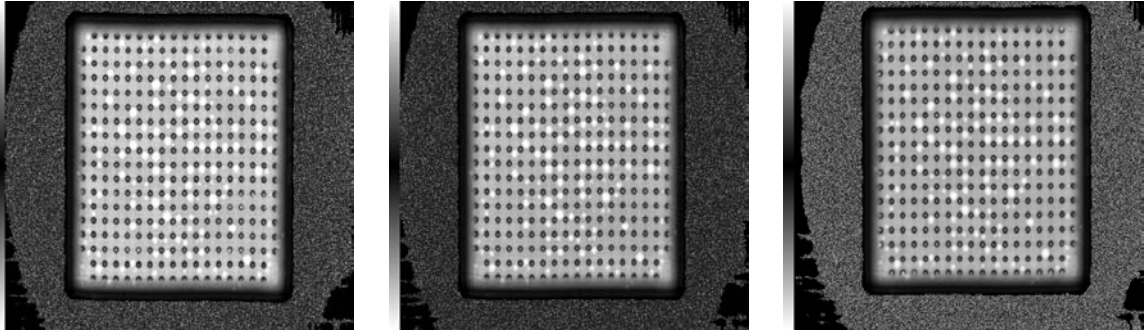


Figure 6-32 FA10 2x2 Ni/Au with TL-Underfill C: CSAM images at 0 cycles (left), 400 cycles, and 900 cycles (right), no delamination

6.1.1.12 FA10 2x2 Ni/Au with TL-Underfill D

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.4. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

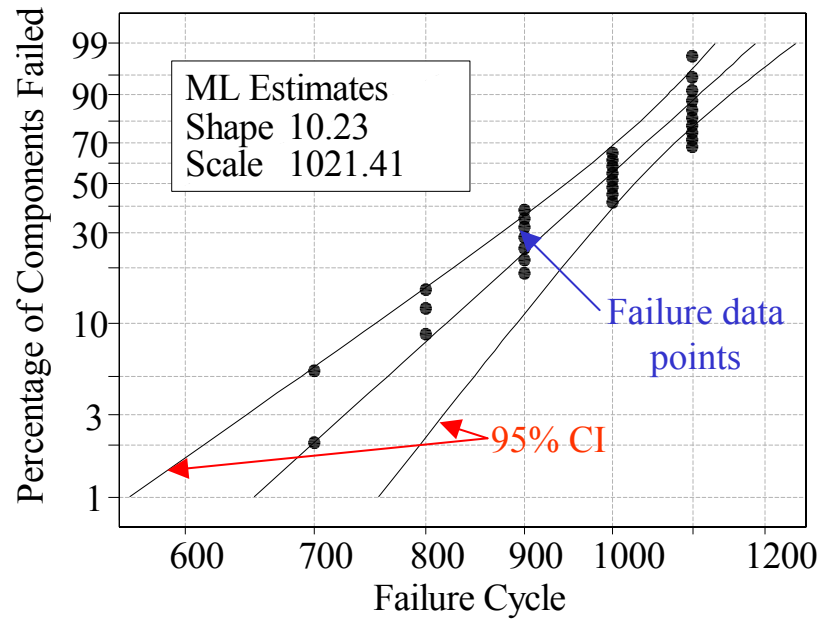


Figure 6-33 Weibull Probability Plot for FA10 2x2 Ni/Au with TL-Underfill D

The mean time to failure for these components was calculated to be 972 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for this test vehicle was at 700 cycles and all parts failed by 1100 cycles. Again, notice the discrepancy in performance between the Ni/Au and OSP substrate metallization test vehicles; Ni/Au with a MTTF of 972 cycles and OSP with a MTTF of 1674 cycles.

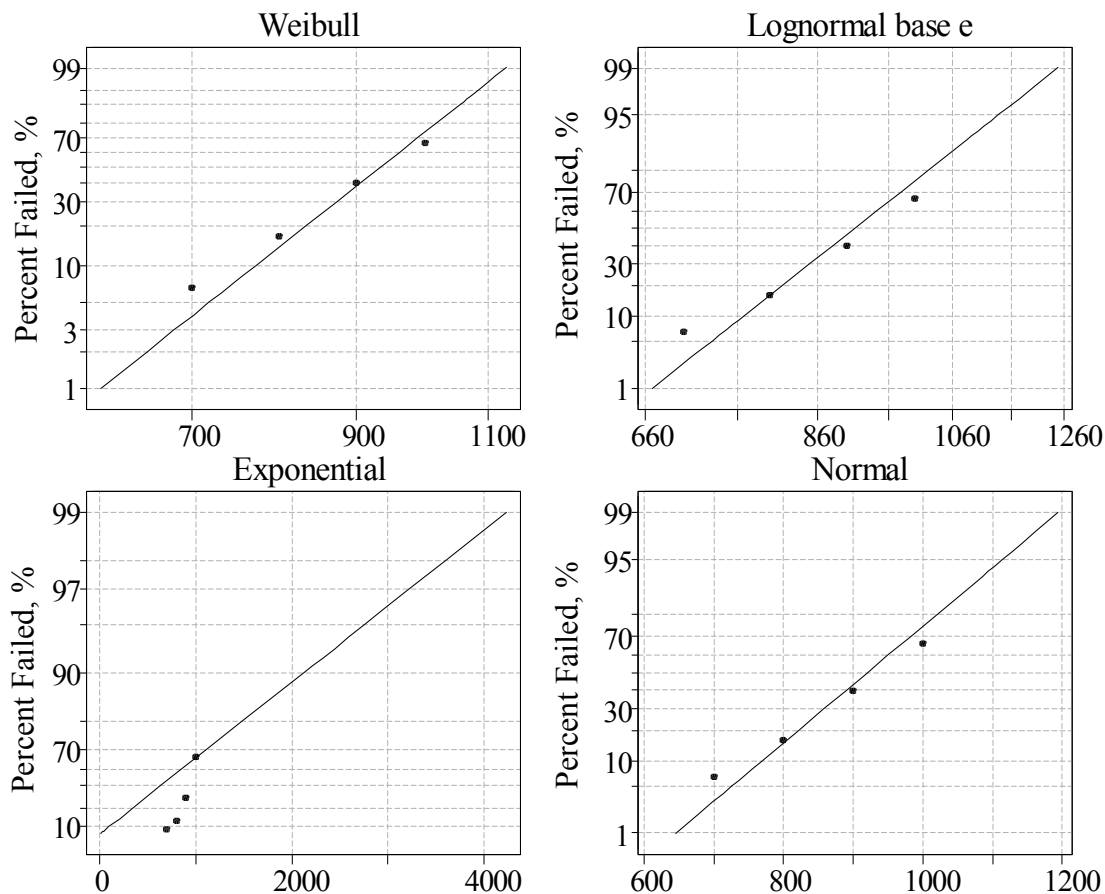


Figure 6-34 Four-Way Probability Plot FA10 2x2 Ni/Au with TL-Underfill D, MLE, Arbitrary Censoring

Table 6-11 Anderson Darling Statistics for FA10 2x2 Ni/Au with TL-Underfill D

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
FA10 2x2 Ni/Au	Underfill D	Weibull	11.69
		Lognormal Base e	11.61
		Exponential	12.46
		Normal	11.56

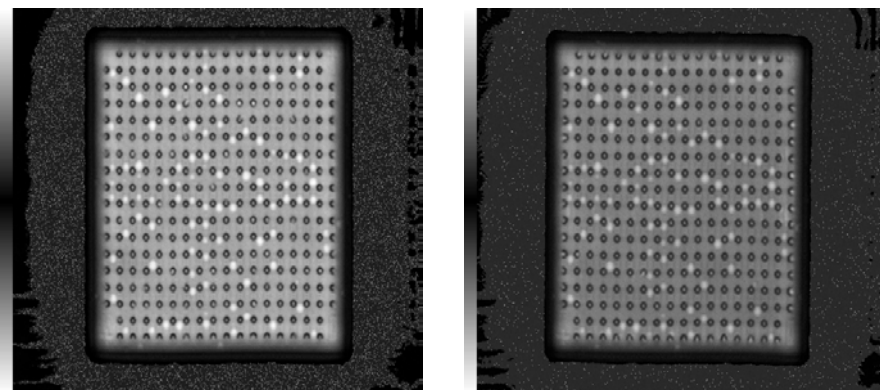


Figure 6-35 FA10 2x2 Ni/Au with TL-Underfill D: CSAM images at 0 cycles (left) and 1100 cycles (right), no delamination

6.1.1.13 FA10 4x4 OSP with Underfill C

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.4. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

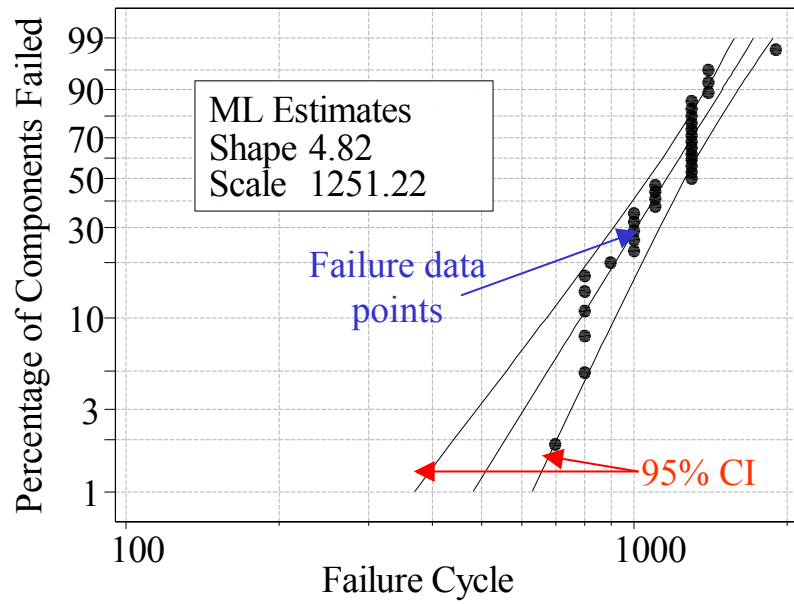


Figure 6-36 Weibull Probability Plot for FA10 4x4 OSP with TL-Underfill C

The mean time to failure for these components was calculated to be 1146 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for this test vehicle was at 700 cycles and all test vehicles failed by 1400 cycles.

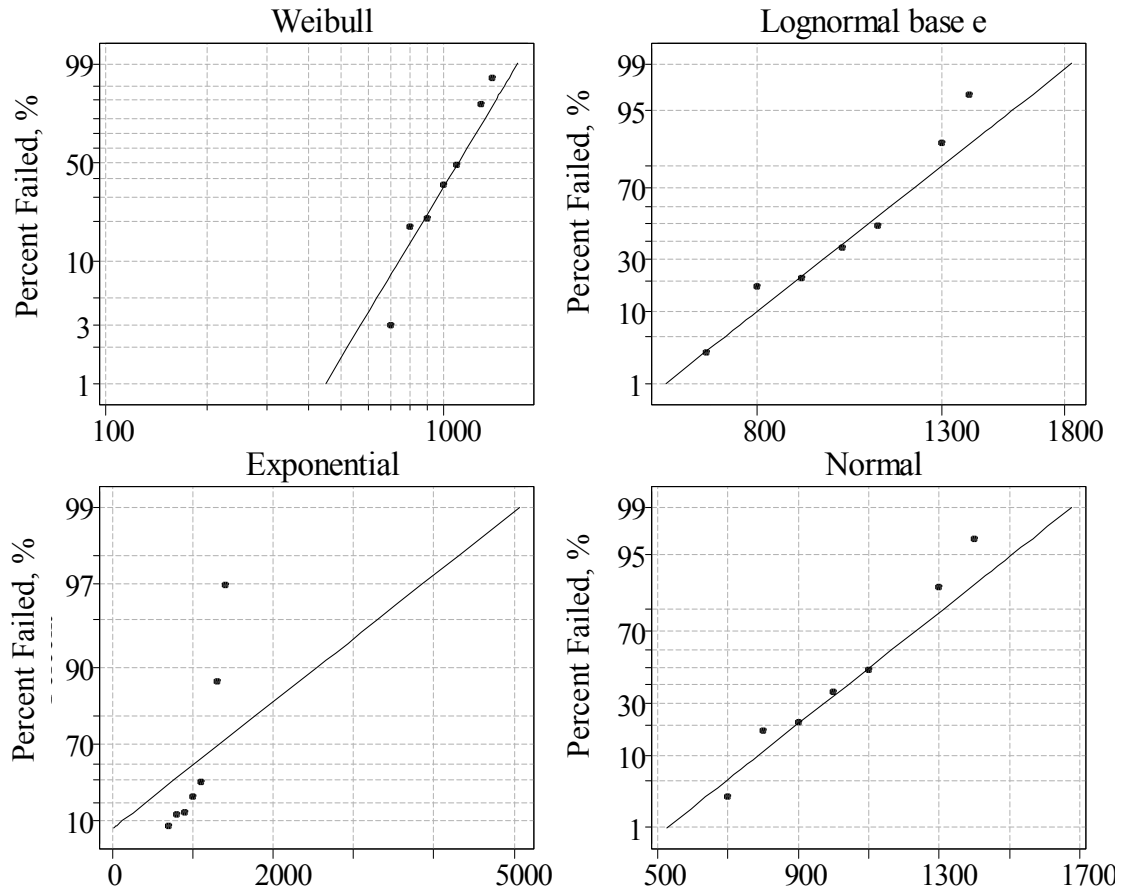


Figure 6-37 Four-Way Probability Plot FA10 4x4 OSP with TL-Underfill C, MLE, Arbitrary Censoring

Table 6-12 Anderson Darling Statistics for FA10 4x4 OSP with TL-Underfill C

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
FA10 4x4 OSP	Underfill C	Weibull	0.540
		Lognormal Base e	0.668
		Exponential	2.257
		Normal	0.582

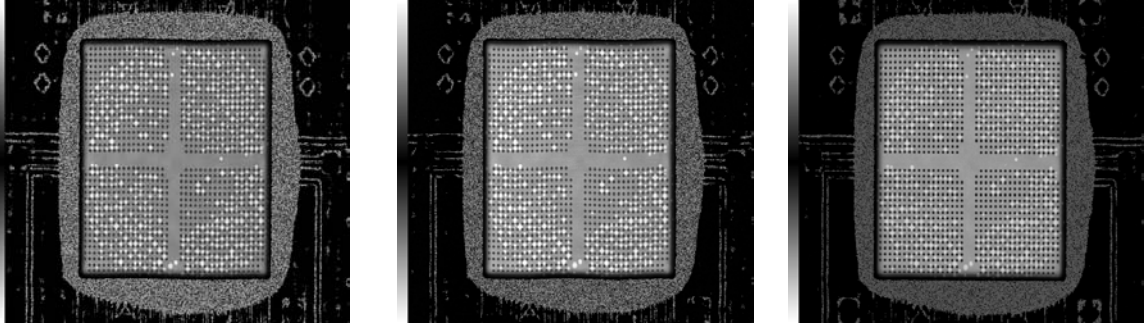


Figure 6-38 FA10 4x4 OSP with TL-Underfill C: CSAM images at 0 cycles (left), 800 cycles, and 1800 cycles (right), no delamination

6.1.1.14 FA10 4x4 OSP with TL-Underfill D

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.4. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

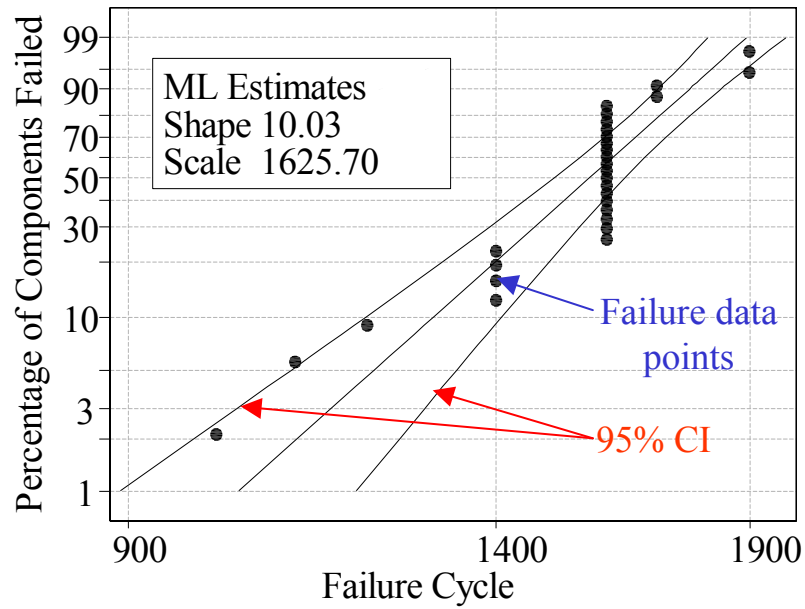


Figure 6-39 Weibull Probability Plot for FA10 4x4 OSP with TL-Underfill D

The mean time to failure for these components was calculated to be 1546 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for this test vehicle was at 1000 cycles and all test vehicles failed by 1900 cycles.

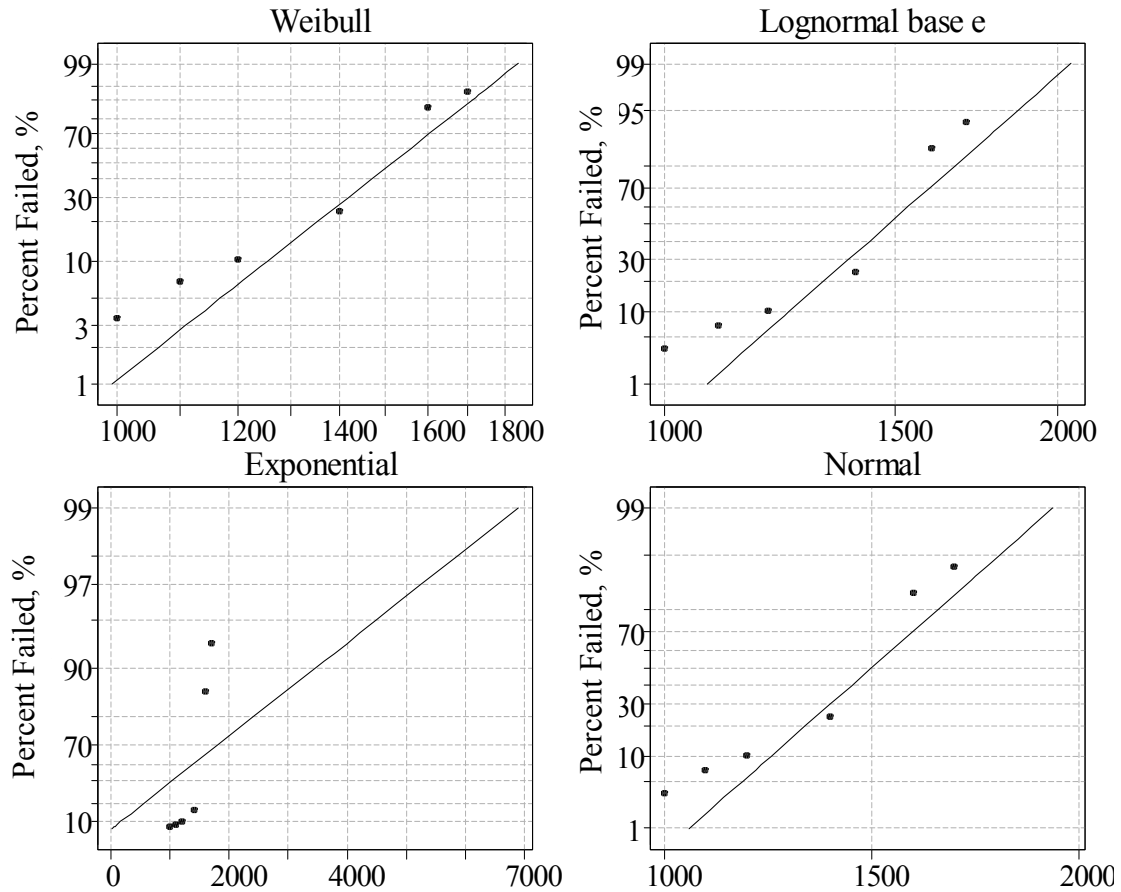


Figure 6-40 Four-Way Probability Plot FA10 4x4 OSP with TL-Underfill D, MLE, Arbitrary Censoring

Table 6-13 Anderson Darling Statistics for FA10 4x4 OSP with TL-Underfill D

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
FA10 4x4 OSP	Underfill D	Weibull	1.554
		Lognormal Base e	1.728
		Exponential	2.796
		Normal	1.677

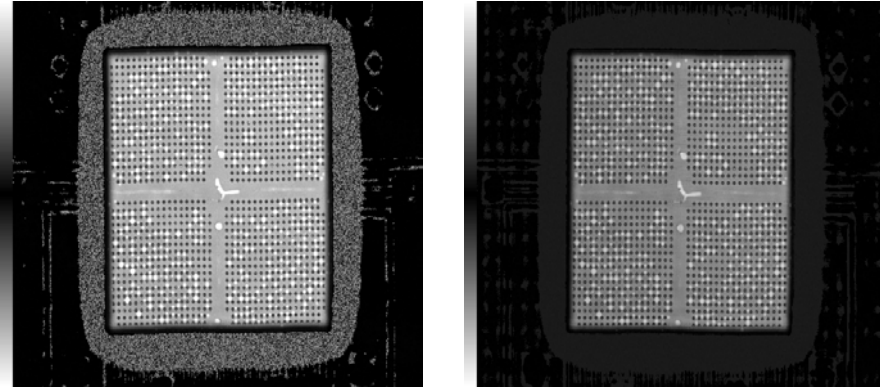


Figure 6-41 FA10 4x4 OSP with TL-Underfill D: CSAM images at 0 cycles (left), 1800 cycles (right), no delamination

6.1.1.15 FA10 4x4 Ni/Au with TL-Underfill C

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.4. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

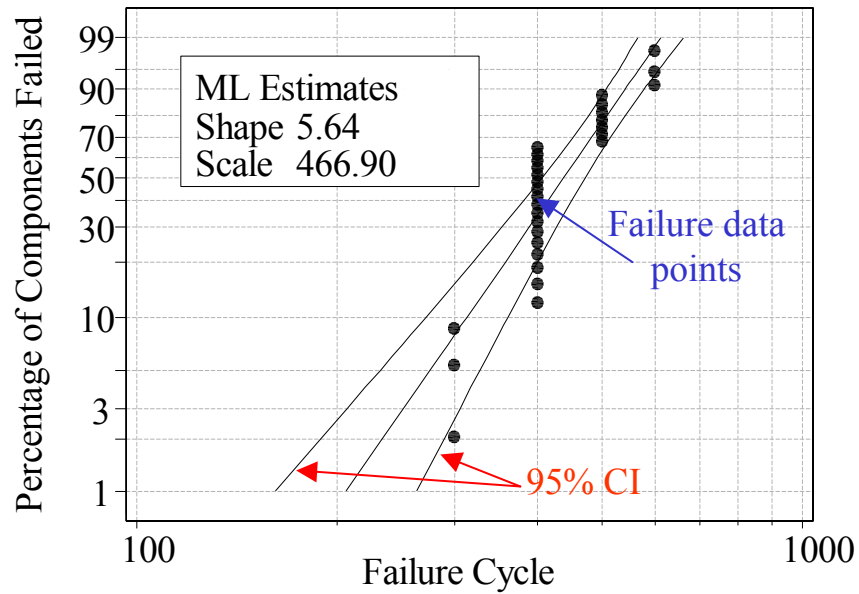


Figure 6-42 Weibull Probability Plot for FA10 4x4 Ni/Au with TL-Underfill C

The mean time to failure for these components was calculated to be 431 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for these components was at 300 cycles and the last failure was at 600 cycles. Again, notice the discrepancy in performance between the Ni/Au and OSP substrate metallization test vehicles; Ni/Au with a MTTF of 431 cycles and OSP with a MTTF of 1146 cycles.

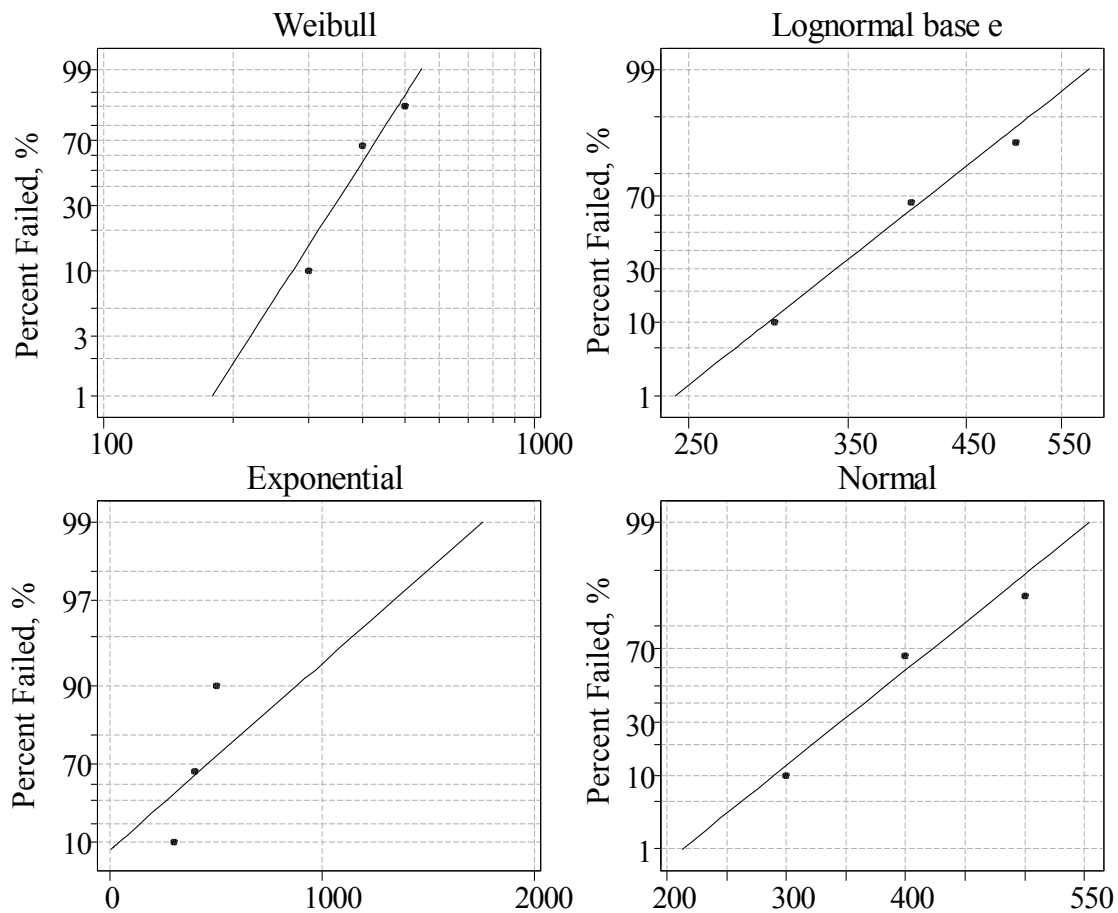


Figure 6-43 Four-Way Probability Plot FA10 4x4 Ni/Au with TL-Underfill C, MLE, Arbitrary Censoring

Table 6-14 Anderson Darling Statistics for FA10 4x4 Ni/Au with TL-Underfill C

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
FA10 4x4 Ni/Au	Underfill C	Weibull	1.383
		Lognormal Base e	1.534
		Exponential	1.800
		Normal	1.458

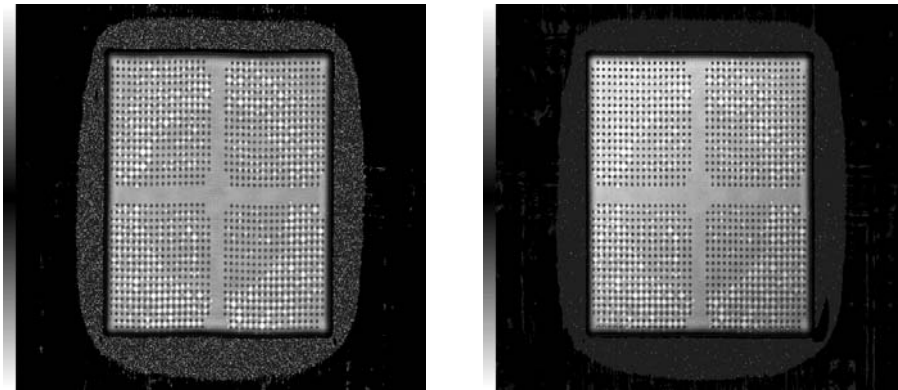


Figure 6-44 FA10 4x4 Ni/Au with TL-Underfill C: CSAM images at 0 cycles (left) and 600 cycles (right), no delamination

6.1.1.16 FA10 4x4 Ni/Au with TL-Underfill D

The reliability data provided in this section was for the test vehicle as described in Section 4.1.1.4. A Weibull probability plot for the AATC failure data was presented; in addition, the shape and the scale parameters are shown in a small box on the probability plot and a 95% confidence interval was plotted. The images in figure show that there was no delamination between the die and the underfill layer as a result of the AATC accelerated life test.

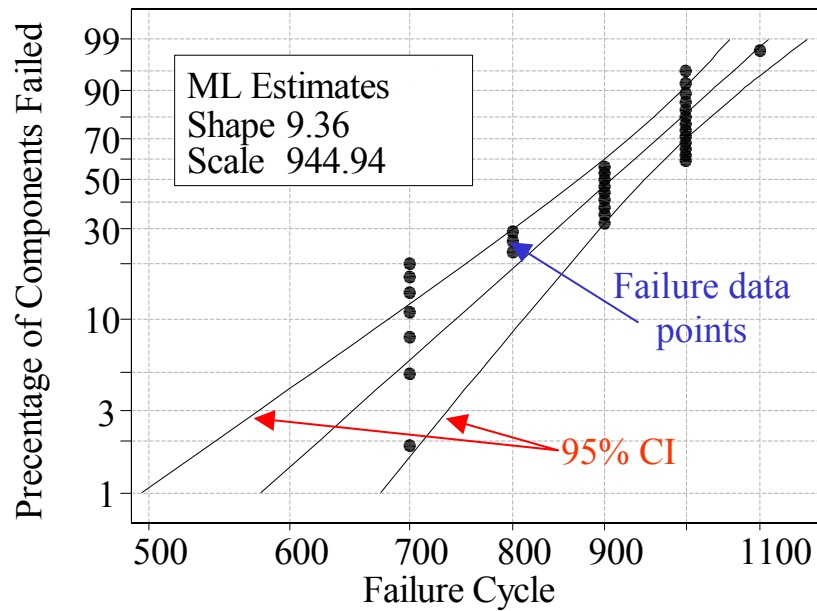


Figure 6-45 Weibull Probability Plot for FA10 4x4 Ni/Au with TL-Underfill D

The mean time to failure for these components was calculated to be 896 cycles; this was calculated via Equation 6-2 in conjunction with the parameter estimates for the shape and the scale factors shown in the figure above. The first failure for these components was at 700 cycles and the last failure was at 1100 cycles. Again, notice the discrepancy in performance between the Ni/Au and OSP substrate metallization test vehicles; Ni/Au with a MTTF of 896 cycles and OSP with a MTTF of 1546 cycles.

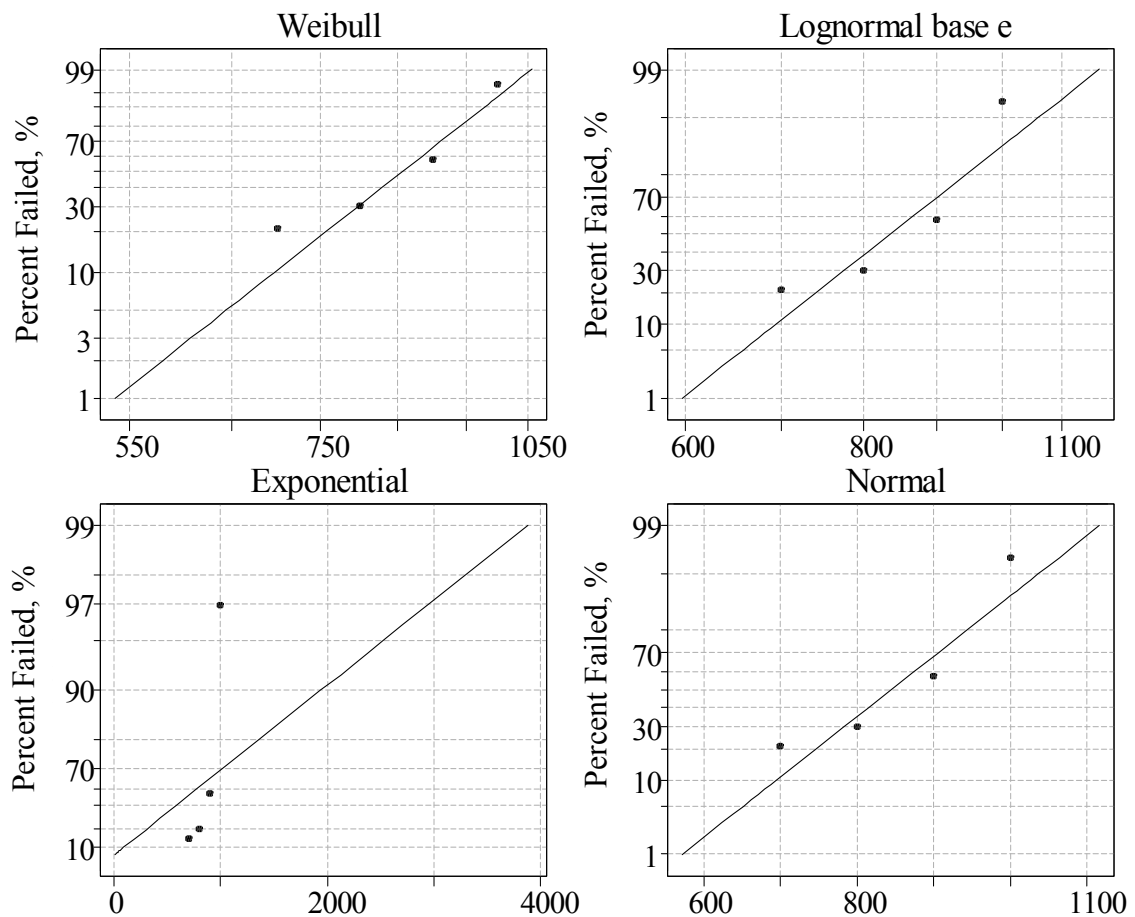


Figure 6-46 Four-Way Probability Plot FA10 4x4 Ni/Au with TL-Underfill D, MLE, Arbitrary Censoring

Table 6-15 Anderson Darling Statistics for FA10 4x4 Ni/Au with TL-Underfill D

Test Vehicle	Underfill	Distribution	Anderson Darling Statistic
FA10 4x4 Ni/Au	Underfill D	Weibull	0.955
		Lognormal Base e	0.799
		Exponential	1.515
		Normal	0.830

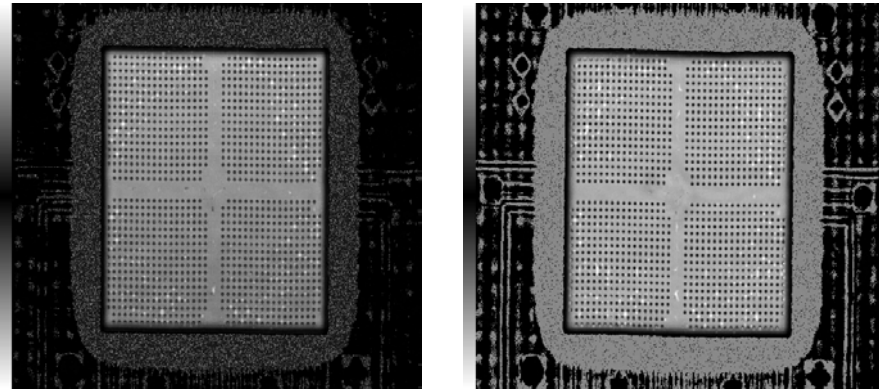


Figure 6-47 FA10 4x4 Ni/Au with TL-Underfill D: CSAM images at 0 cycles (left) and 1000 cycles (right), no delamination

6.1.1.17 Summary of the AATC reliability statistics

Notice that the samples made with TL-Underfill D outperformed the samples made with TL-Underfill C, with a difference in MTTF of 273 cycles. The performance shift due to underfill material is suspected to be a result of the difference in the glass transition temperatures between TL-Underfill C and TL-Underfill D. The glass transition temperature of TL-Underfill C was 62 °C as opposed to 88 °C for TL-Underfill D.

There was a distinct shift in performance between the PB6 and the PB8 test vehicles in terms of reliability performance. The reason for this shift is the difference in solder joint shape. As you can see from the optical images of the bond pads; the PB8 bond pads arranged horizontally are SMD on two sides and NSMD on the other two sides and the bond pads that are arranged vertically are SMD on three sides and NSMD on only one side of the bond pad. Notice that the PB6 bond pads have better mask alignment which results in all pads being SMD on two sides of the bond pads and NSMD on the other two sides of the bond pads.

Individual
bond pad

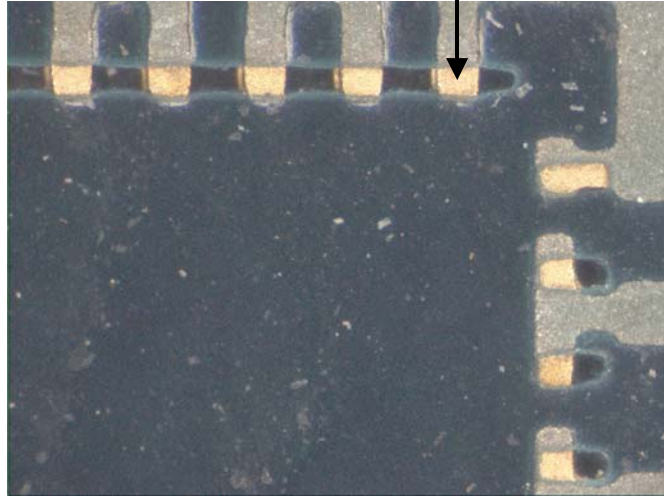


Figure 6-48 Optical Images of PB8 Bond Pads

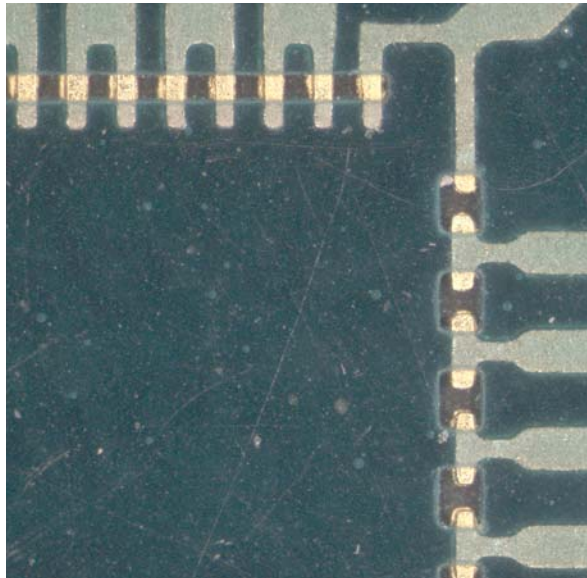


Figure 6-49 Optical Images of PB6 bond pads

Neither the PB6 nor the PB8 exhibited superior reliability performance mainly because the solder mask openings were rather small in comparison to the FA10 mask openings and resulting wettable pad area. The area ratio, which was the UBM area to the

wettable pad area, was plotted for the various test vehicles in the box plot shown in Figure 6-51. There were 60 pad area measurements taken for the three test vehicles; 30 measurements were taken for both the OSP and Ni/Au substrate metallizations. There was no significant difference in the wettable pad areas between the substrate metallizations; therefore the data from the two metallizations was combined for the purposes of plotting the areas in Figure 6-51. There was not only a large difference in the area ratios between the perimeter and the area array test vehicles but there was also a large amount of variation in the pad areas. This meant that the chances of getting a very small pad were greater for the perimeter array test vehicles. This could result in a joint that was weak initially due to poor solder joint shape. Solder joints with very small wettable pad areas often fractured at the substrate side of the die when placed in AATC testing. An example of the failure mechanism seen as a result of a very small wettable pad area is shown in the figure below.

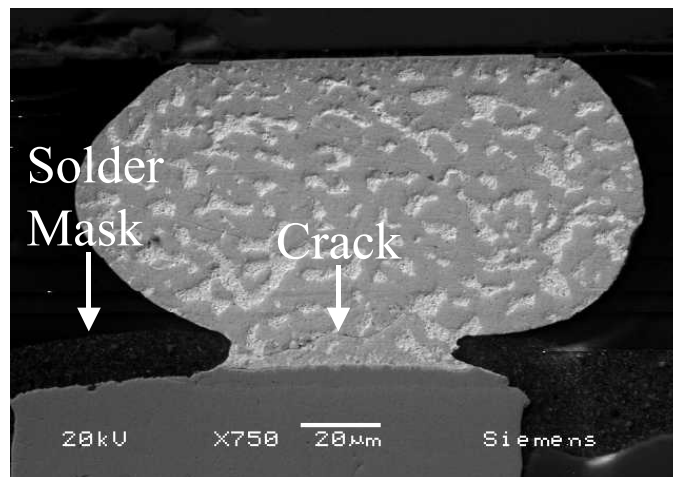


Figure 6-50 PB8 2x2 Ni/Au: Poor solder joint shape and potential crack at bottom of joint

[F10 #1]

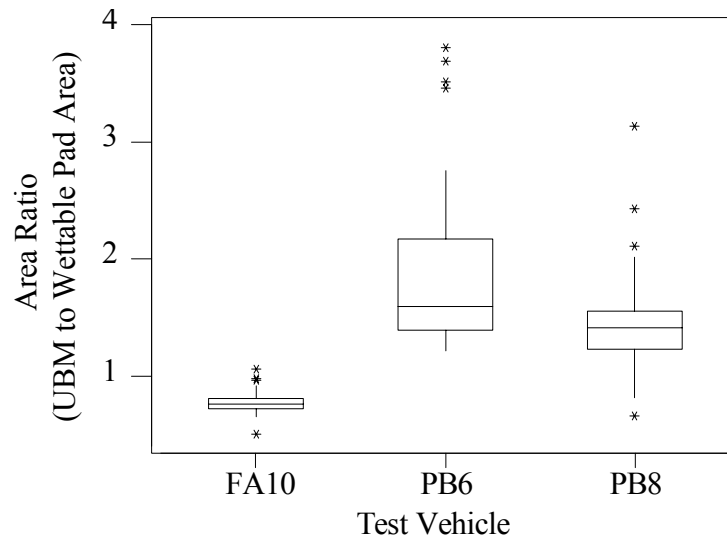


Figure 6-51 Area ratio vs. Test Vehicle Box Plot to Show the Difference in the Size of Solder Mask Openings on the Various Substrates

It is worth mentioning that the performance of this underfill material in HAST (Highly Accelerated Stress Test) was not acceptable, the underfill material actually ran out from under the die during the test resulting in images such as the one shown in Figure 6-52 below; the remainder of the HAST failure data was presented by Lazarakis [Lazarakis, 2003]. This same behavior was demonstrated by all test vehicles that were tested in HAST: PB6, PB8, FA10 2x2 and FA10 4x4.

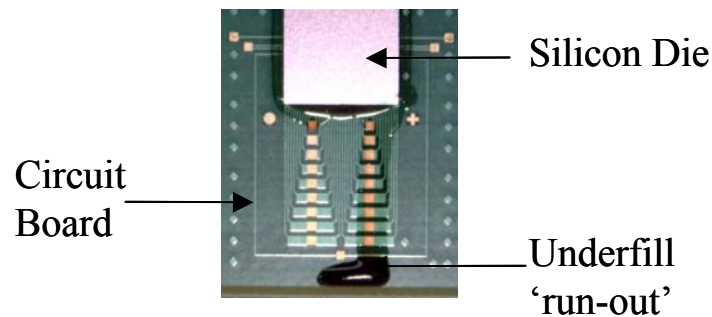


Figure 6-52 Example of TL-Underfill D Material Performance in HAST

Table 6-16 AATC Reliability Statistics

Test Vehicle	Underfill	Weibull Shape	Weibull Scale	Cycles to First Failure	Cycles to Last Failure	MTTF as calculated via Equation 6-2
PB8 2x2 OSP	TL-Underfill C	11.10	386.36	300	400	368
	TL-Underfill D	5.92	397.58	300	500	368
PB8 2x2 Ni/Au	TL-Underfill C	3.49	248.37	100	300	223
	TL-Underfill D	3.69	262.28	100	400	236
PB6 2x2 OSP	TL-Underfill C	7.16	558.76	300	700	523
	TL-Underfill D	6.92	852.06	500	1000	796
PB6 2x2 Ni/Au	TL-Underfill C	6.12	303.24	200	400	281
	TL-Underfill D	5.85	570.34	300	700	528
FA10 2x2 OSP	TL-Underfill C	5.30	2627.34	1700	3500	2420
	TL-Underfill D	5.41	1814.74	1100	2300	1674
FA10 2x2 Ni/Au	TL-Underfill C	3.25	656.11	300	900	588
	TL-Underfill D	10.23	1021.41	700	1100	972
FA10 4x4 OSP	TL-Underfill C	4.83	1251.22	700	1400	1146
	TL-Underfill D	10.03	1625.70	1000	1900	1546
FA10 4x4 Ni/Au	TL-Underfill C	5.64	466.90	300	600	431
	TL-Underfill D	9.37	944.94	700	1100	896

6.1.2 Test Data on Additional Test Vehicles (used in Regression Analysis)

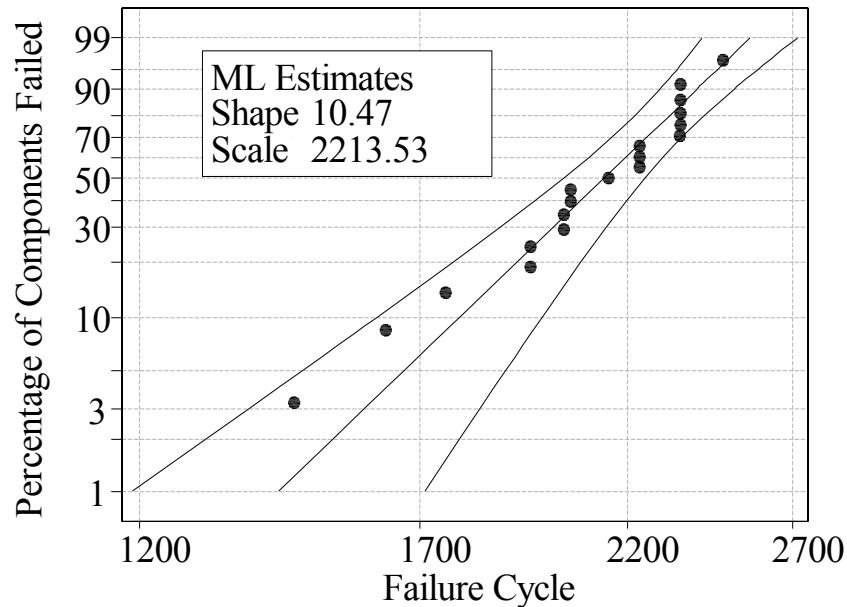


Figure 6-53 AATC Failure Data for FA10 2x2 on Siemens Boards; Colella Underfill B [-55 to 125°C]

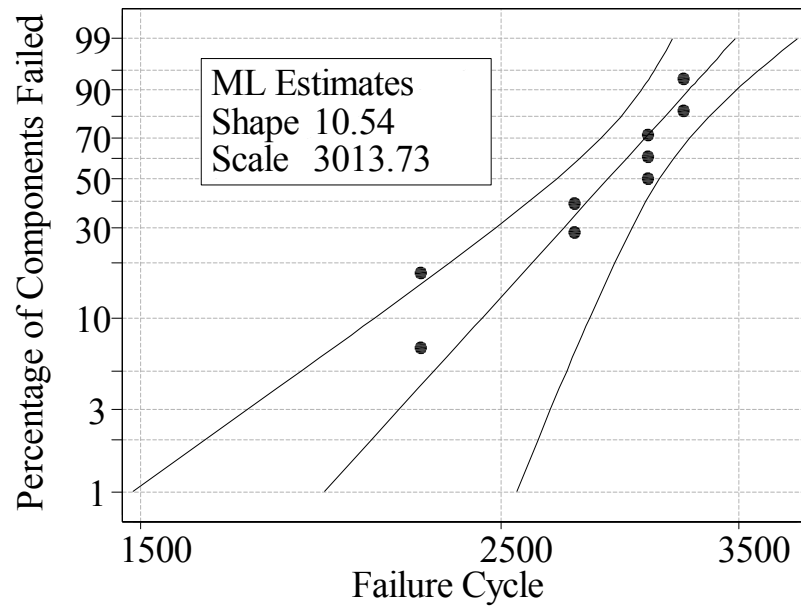


Figure 6-54 AATC Failure Data for FA10 2x2 on Siemens Boards; Colella Underfill A [-
55 to 125°C]

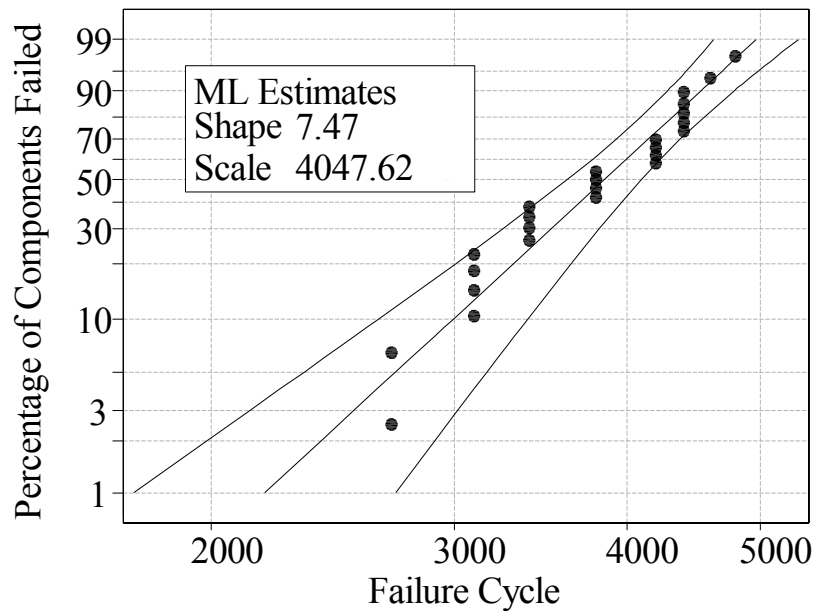


Figure 6-55 AATC Failure Data for FA10 2x2 on Siemens AG Boards; Colella Underfill
B [-40 to 125°C]

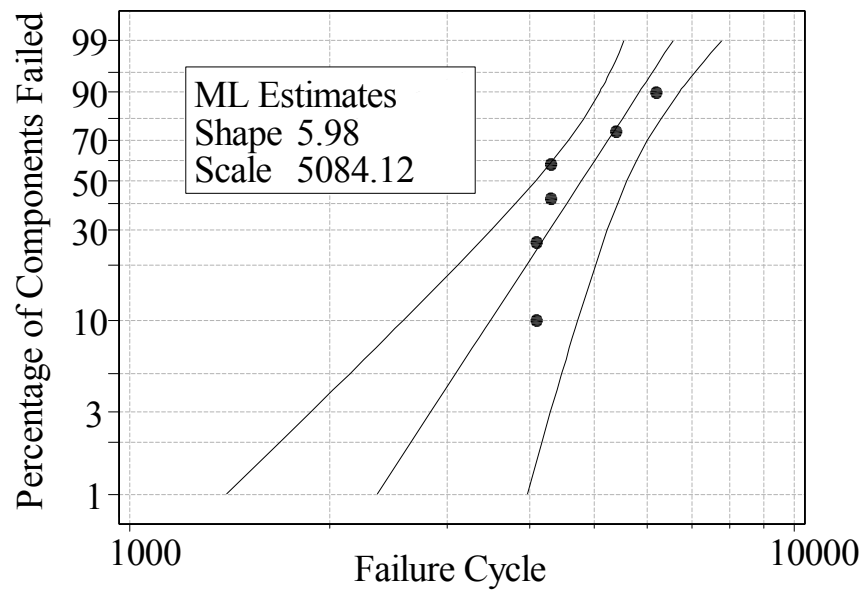


Figure 6-56 AATC Failure Data for FA10 2x2 on Siemens AG Boards; Colella Underfill

B [-55 to 125°C]

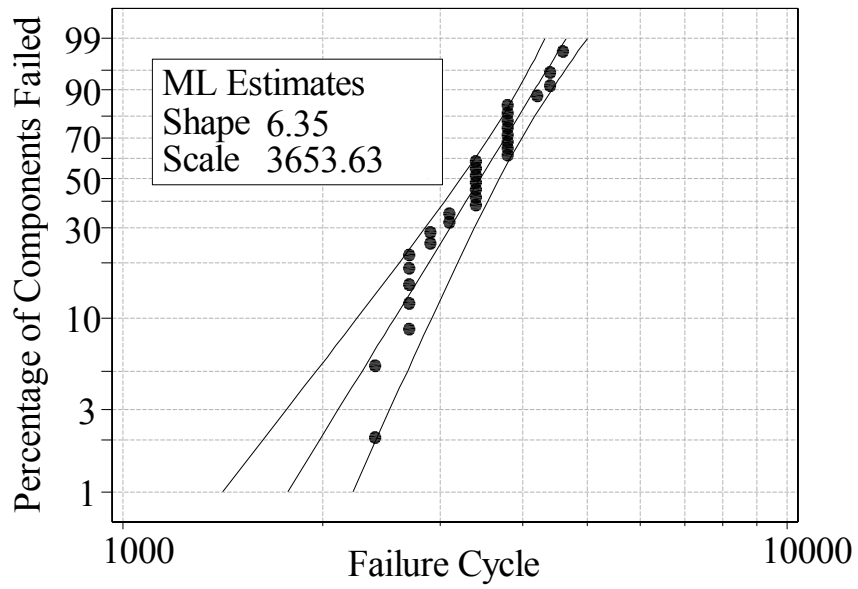


Figure 6-57 AATC Failure Data for FA10 2x2 on Siemens AG Boards; Colella Underfill

E [-40 to 125°C]

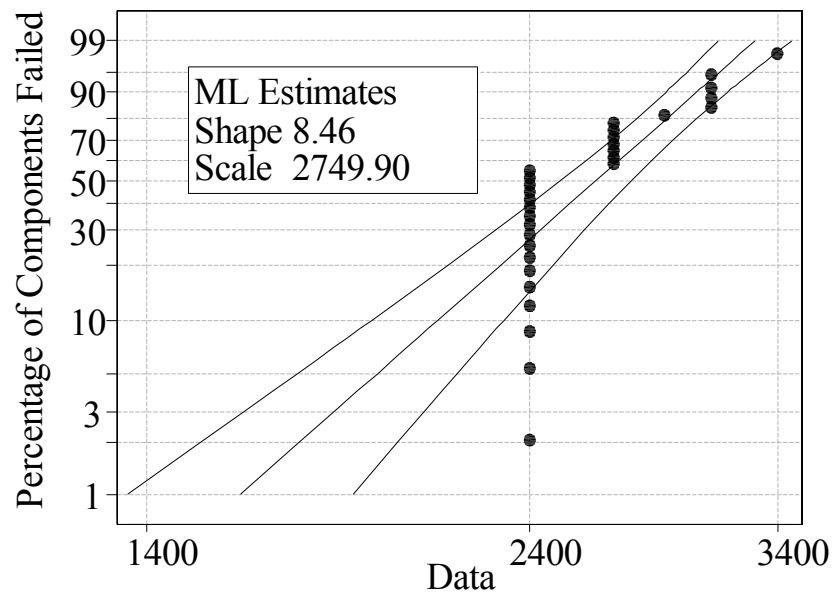


Figure 6-58 AATC Failure Data for FA10 2x2 on Siemens AG Boards; Colella Underfill

C [-40 to 125°C]

6.1.3 High Temperature Storage

A high temperature storage test, HTS, was performed on 509 total flip chip on board samples, details of the test vehicles placed in the HTS test are shown in Table 6-17. The high temperature storage test basically consists of placing the components into an isothermal condition for several hundred hours and then monitoring the performance of the components at interval readouts. High temperature storage condition B was run which is 150°C for 1000 hours; specification JESD22-A103-B. The integrity of the electrical interconnects was verified with a two point resistance measurement at interval readouts every 200 hours. A change in resistance by $\pm 10\%$ was considered to be an electrical failure. In addition, scanning acoustic microscopy was used to inspect for underfill delamination. The scanning acoustic microscopy was performed every 200 cycles on a sample lot from each test configuration.

6.1.3.1 FA10 2x2 Siemens HTS Results

The High Temperature Storage reliability data provided in this section was for the test vehicle as described in Section 4.1.1.3. A summary of the test vehicle performance is shown in the table below. The results are presented on a pass/fail basis for the High Temperature Storage Test as described in the JEDEC specification JESD22-A103-B, condition B. The integrity of the solder interconnects was determined via electrical continuity testing at 200 cycle intervals. If the components passed the test, the result of the test would be 'Passed' and the comments would be '1000 hours' indicating the last time that the parts were evaluated. If the components failed any of the electrical continuity readouts prior to 1000 hours, the result of the test would be 'Fail' and the

comments section shows at what readout the components failed. The CSAM images in figure show that there was no delamination between the die and the underfill layer as a result of the HTS accelerated life test.

Table 6-17 HTS Results for FA10 2x2 Siemens Test Vehicles

Test Die & Board	Substrate Metallization	TI - Underfill Material	Board #	# of Parts Tested	Result of HTS Test [150oC, 1000 hours]	Comments
FA10 2x2 (Siemens): Test Vehicle Described in Section 4.1.1.3	Cu/Ni/Au	C	F07	10	Fail	100% failed at 800 hours
			F08	9	Fail	100% failed at 800 hours
		D	F30	10	Fail	100% failed at 800 hours
			F27	9	Fail	100% failed at 800 hours

The FA10 2x2 Siemens test vehicles failed the high temp storage life test. All samples failed electrically at the 800 cycle readout. Since interval readouts were used the exact failure time was not determined; however, 100% of the components failed between 600 and 800 hours. Again, these failures are electrical failures where to electrical resistance of the net changed by $\pm 10\%$ from the initial resistance value that was taken prior to any accelerated life testing.

6.1.3.2 PB6 2x2 HTS Results (OSP & Ni/Au : TL-Underfill C & TL-Underfill D)

The High Temperature Storage reliability data provided in this section was for the test vehicle as described in Section 4.1.1.2. A summary of the test vehicle performance is shown in the table below. The results are presented on a pass/fail basis for the High Temperature Storage Test as described in the JEDEC specification JESD22-A103-B, condition B. The integrity of the solder interconnects was determined via electrical continuity testing at 200 cycle intervals. If the components passed the test, the result of the test would be 'Passed' and the comments would be '1000 hours' indicating the last time that the parts were evaluated. If the components failed any of the electrical continuity readouts prior to 1000 hours, the result of the test would be 'Fail' and the comments section shows at what readout the components failed. The CSAM images in figure show that there was no delamination between the die and the underfill layer as a result of the HTS accelerated life test.

Table 6-18 HTS Results for PB6 2x2 Test Vehicles

Test Die & Board	Substrate Metallization	TL - Underfill Material	Board #	# of Parts Tested	Result of HTS Test [150oC, 1000 hours]	Comments
PB6 2x2: Test Vehicle Described in Section 4.1.1.2	Cu/Ni/Au	C	F07	10	Fail	100% failed at 800 hours
			F10	10	Fail	100% failed at 800 hours
			F12	11	Fail	100% failed at 800 hours
		D	F27	11	Fail	100% failed at 800 hours
			F28	11	Fail	100% failed at 800 hours
			F32	12	Fail	1 failed at 400, 11 at 800 hours
	Cu/OSP	C	F13	12	Passed	1000 hours
			F14	12	Passed	1000 hours
			F15	12	Passed	1000 hours
		D	F28	11	Passed	1000 hours
			F31	12	Passed	1000 hours
			F32	12	Passed	1000 hours

All of the PB6 2x2 Ni/Au samples failed the high temperature storage life test and all of the PB6 2x2 OSP samples passed 1000 of high temperature storage life testing at 150 °C for 1000 hours.

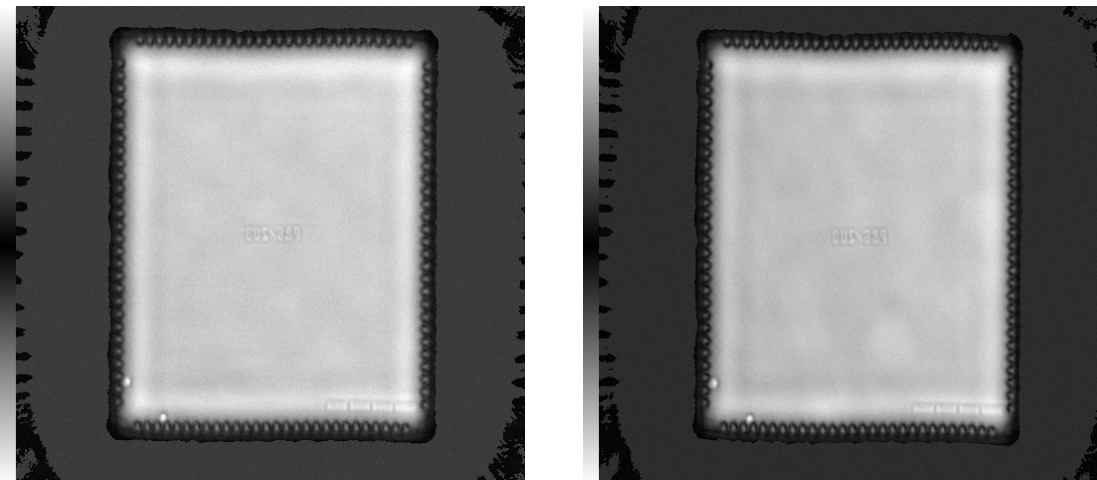


Figure 6-59 CSAM images at 0 hours (left) and 800 hours (right);no delamination;
PB62x2 Ni/Au TL-Underfill C, Board Number F12

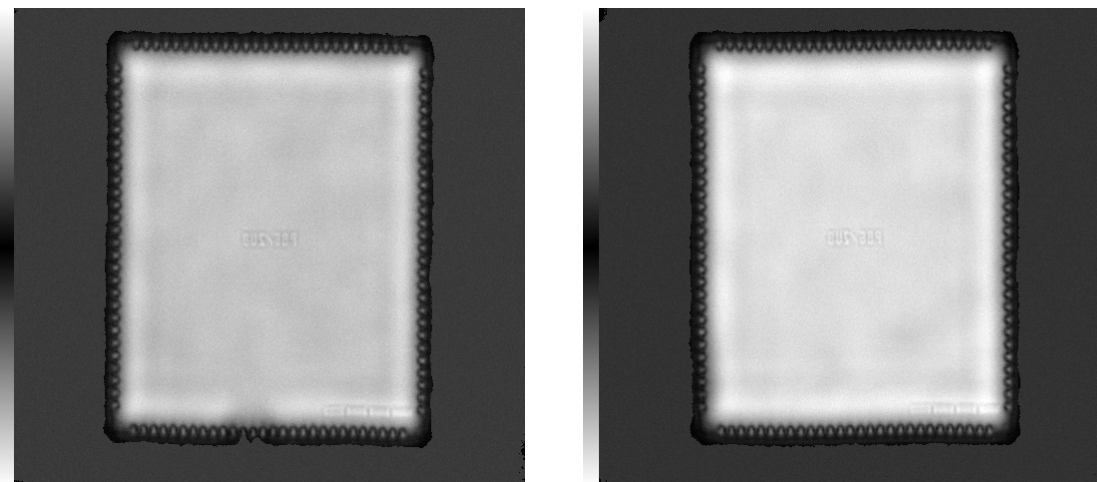


Figure 6-60 CSAM images at 0 hours (left) and 800 hours (right);no delamination;
PB62x2 Ni/Au TL-Underfill D, Board Number F32

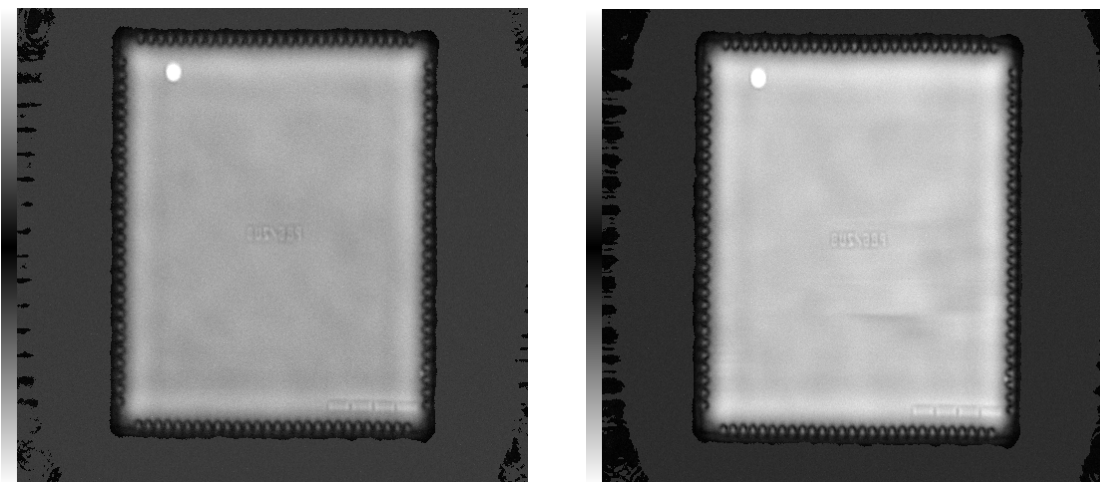


Figure 6-61 CSAM images at 0 hours (left) and 800 hours (right);no delamination;

PB62x2 OSP TL-Underfill C, Board Number F15

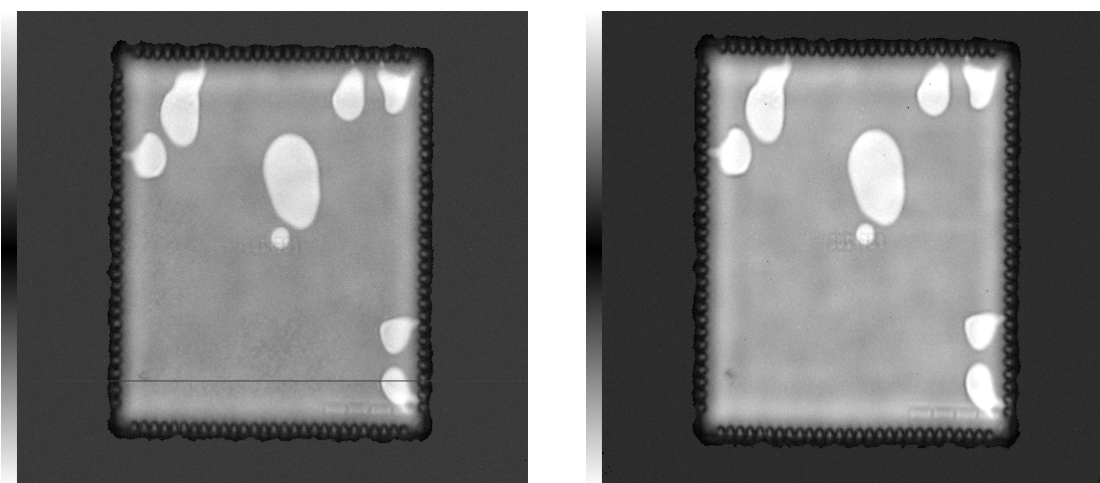


Figure 6-62 CSAM images at 0 hours (left) and 800 hours (right);no delamination;

PB62x2 OSP TL-Underfill D, Board Number F32

6.1.3.3 PB8 2x2 HTS Results (OSP & Ni/Au : TL-Underfill C & TL-Underfill D)

The High Temperature Storage reliability data provided in this section was for the test vehicle as described in Section 4.1.1.1. A summary of the test vehicle performance is shown in the table below. The results are presented on a pass/fail basis for the High

Temperature Storage Test as described in the JEDEC specification JESD22-A103-B, condition B. The integrity of the solder interconnects was determined via electrical continuity testing at 200 cycle intervals. If the components passed the test, the result of the test would be 'Passed' and the comments would be '1000 hours' indicating the last time that the parts were evaluated. If the components failed any of the electrical continuity readouts prior to 1000 hours, the result of the test would be 'Fail' and the comments section shows at what readout the components failed. The CSAM images in figure show that there was no delamination between the die and the underfill layer as a result of the HTS accelerated life test.

Table 6-19 HTS Results for PB8 2x2 Test Vehicles

Test Die & Board	Substrate Metallization	TL - Underfill Material	Board #	# of Parts Tested	Result of HTS Test [150oC, 1000 hours]	Comments
PB8 2x2: Test Vehicle Described in Section 4.1.1.1	Cu/Ni/Au	C	F13	11	Fail	100% failed at 800 hours
			F14	11	Fail	100% failed at 800 hours
			F15	10	Fail	100% failed at 800 hours
		D	F32	7	Passed	1000 hours
			F30	7	Fail	6 failed at 800, 1 at 1000
			F28	9	Passed	1000 hours
	Cu/OSP	C	F06	10	Passed	1000 hours
			F12	11	Passed	1000 hours
			F15	11	Passed	1000 hours
		D	F25	10	Passed	1000 hours
			F27	11	Passed	1000 hours
			F34	11	Passed	1000 hours

All of the PB8 2x2 Ni/Au samples with underfill Material C failed the high temperature storage life test and 7 out of 23 samples with Material D failed. All of the PB8 2x2 OSP samples passed high temperature storage life testing at 150 °C for 1000 hours.

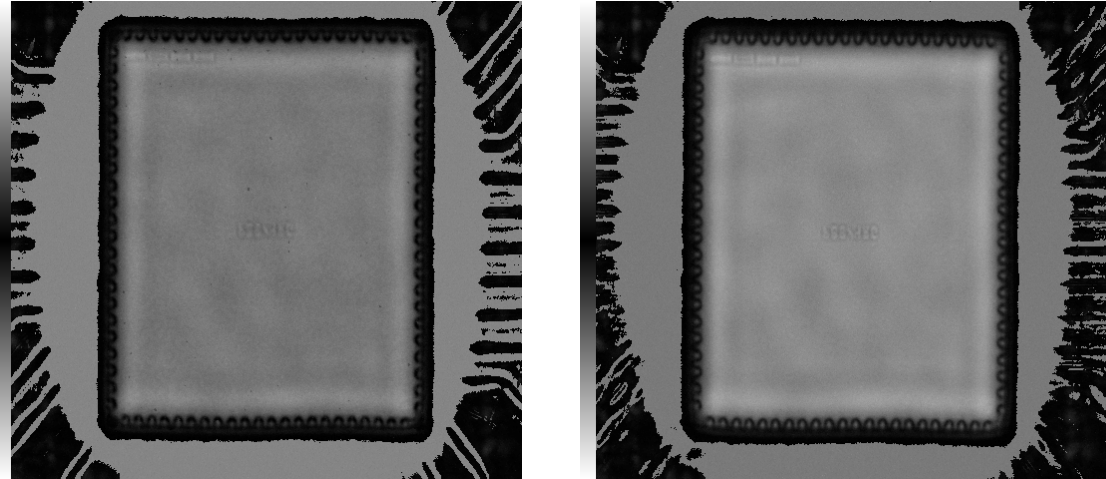


Figure 6-63 CSAM images at 0 hours (left) and 800 hours (right);no delamination;

PB82x2 Ni/Au TL-Underfill C, Board Number F14

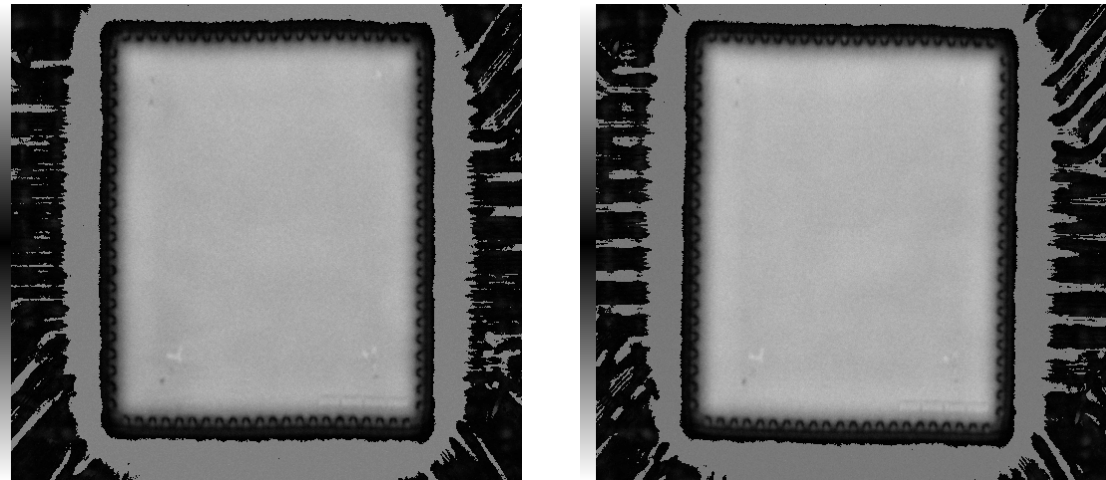


Figure 6-64 CSAM images at 0 hours (left) and 800 hours (right);no delamination;

PB82x2 Ni/Au TL-Underfill D, Board Number F28

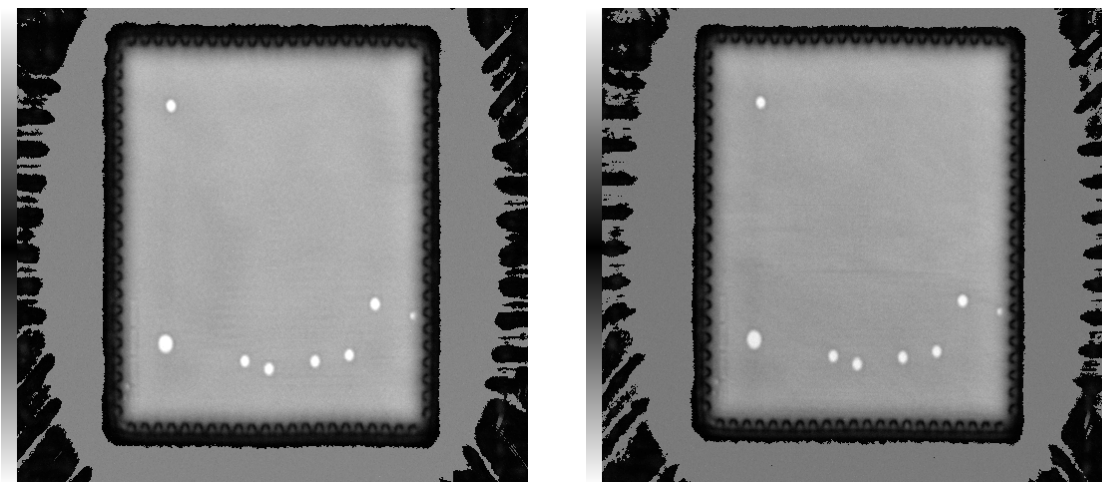


Figure 6-65 CSAM images at 0 hours (left) and 800 hours (right);no delamination;
PB82x2 OSP TL-Underfill C, Board Number F15

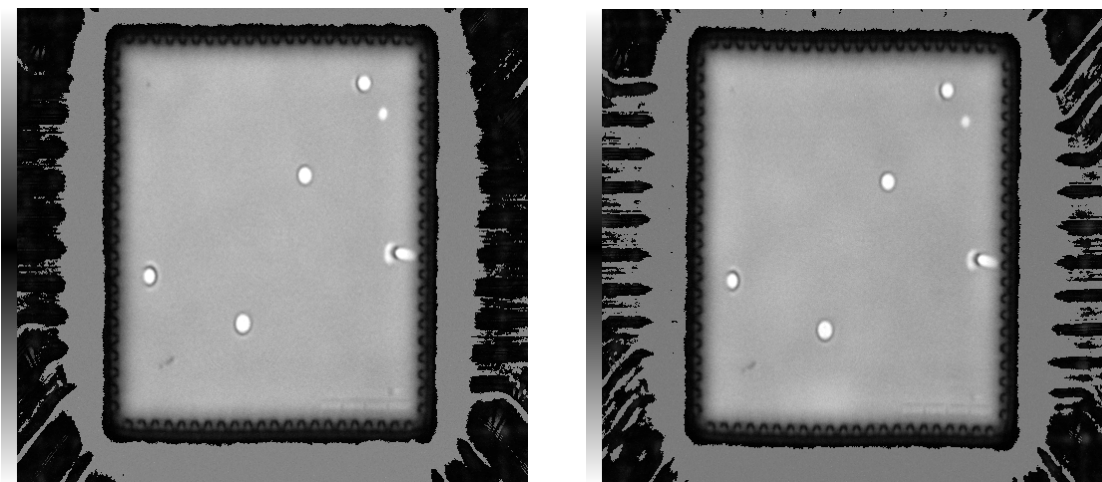


Figure 6-66 CSAM images at 0 hours (left) and 800 hours (right);no delamination;
PB82x2 OSP TL-Underfill D, Board Number F34

6.1.3.4 FA10 2x2 HTS Results (OSP & Ni/Au : TL-Underfill C & TL-Underfill D)

The High Temperature Storage reliability data provided in this section was for the test vehicle as described in Section 4.1.1.4. A summary of the test vehicle performance is shown in the table below. The results are presented on a pass/fail basis for the High

Temperature Storage Test as described in the JEDEC specification JESD22-A103-B, condition B. The integrity of the solder interconnects was determined via electrical continuity testing at 200 cycle intervals. If the components passed the test, the result of the test would be 'Passed' and the comments would be '1000 hours' indicating the last time that the parts were evaluated. If the components failed any of the electrical continuity readouts prior to 1000 hours, the result of the test would be 'Fail' and the comments section shows at what readout the components failed. The CSAM images in figure show that there was no delamination between the die and the underfill layer as a result of the HTS accelerated life test.

Table 6-20 HTS Results for FA10 2x2 Test Vehicles

Test Die & Board	Substrate Metallization	TL - Underfill Material	Board #	# of Parts Tested	Result of HTS Test [150oC, 1000 hours]	Comments
FA10 2x2 : Test Vehicle Description in Section 4.1.1.4	Cu/Ni/Au	C	F08	9	Fail	100% failed at 800 hours
			F13	9	Fail	100% failed at 800 hours
			F14	10	Fail	100% failed at 800 hours
		D	F28	9	Fail	100% failed at 800 hours
			F31	10	Fail	100% failed at 800 hours
			F32	10	Fail	100% failed at 800 hours
	Cu/OSP	C	F10	9	Passed	1000 hours
			F12	9	Passed	1000 hours
			F13	9	Passed	1000 hours
		D	F30	10	Passed	1000 hours
			F31	10	Passed	1000 hours
			F34	9	Passed	1000 hours

All of the FA10 2x2 Ni/Au samples failed the high temperature storage life test and all of the FA10 2x2 OSP samples passed 1000 of high temperature storage life testing at 150 °C for 1000 hours.

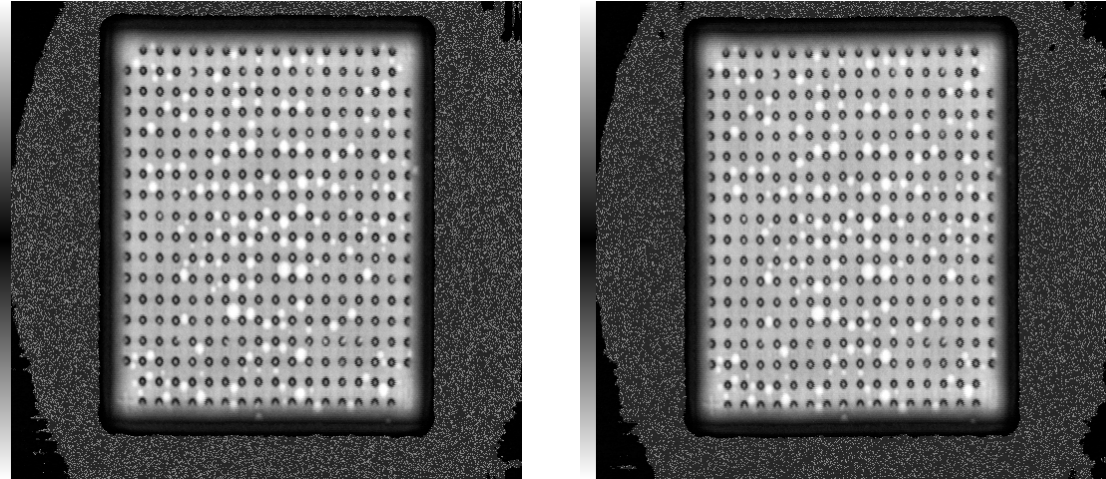


Figure 6-67 CSAM images at 0 hours (left) and 800 hours (right);no delamination;

FA102x2 Ni/Au TL-Underfill C, Board Number F14

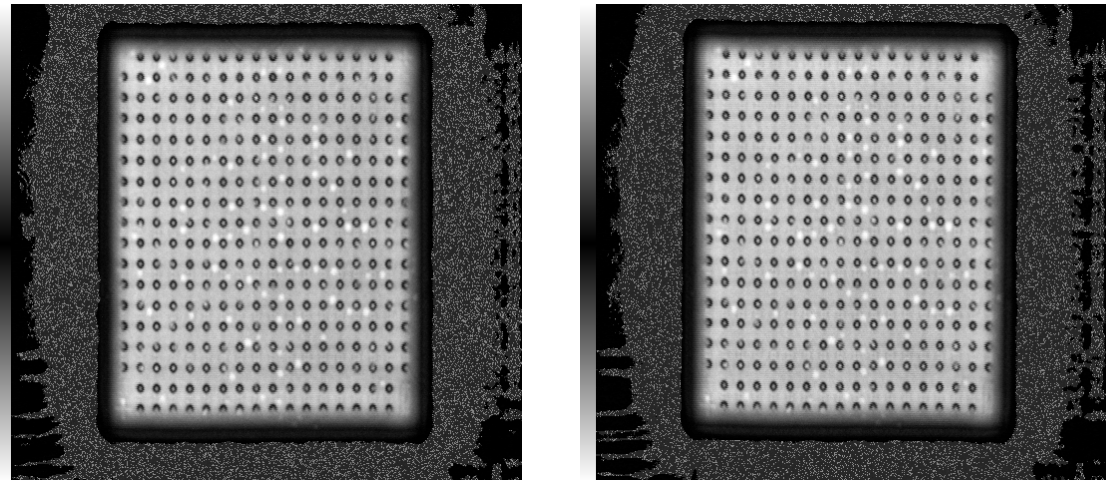


Figure 6-68 CSAM images at 0 hours (left) and 800 hours (right);no delamination;

FA102x2 Ni/Au TL-Underfill D, Board Number F31

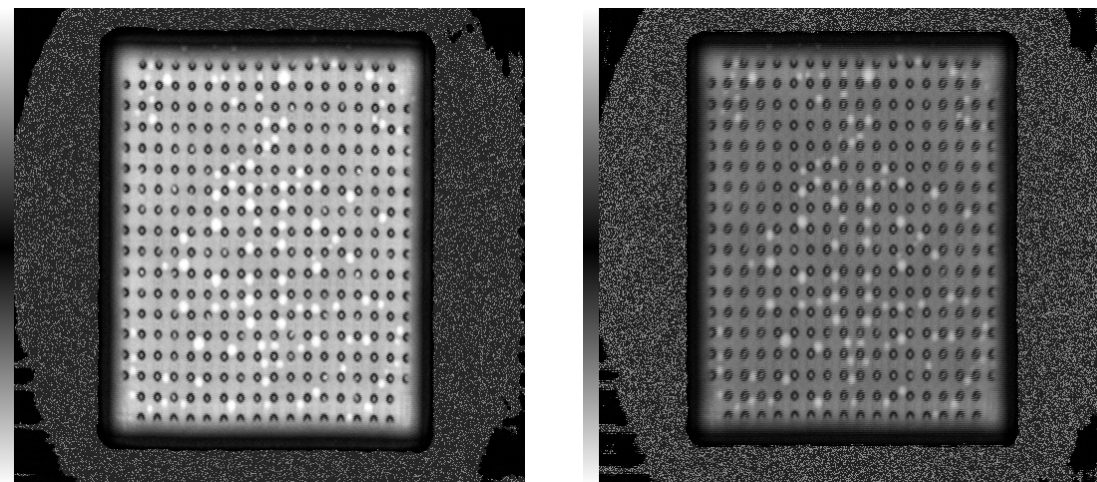


Figure 6-69 CSAM images at 0 hours (left) and 1000 hours (right);no delamination;

FA102x2 OSP TL-Underfill C, Board Number F13

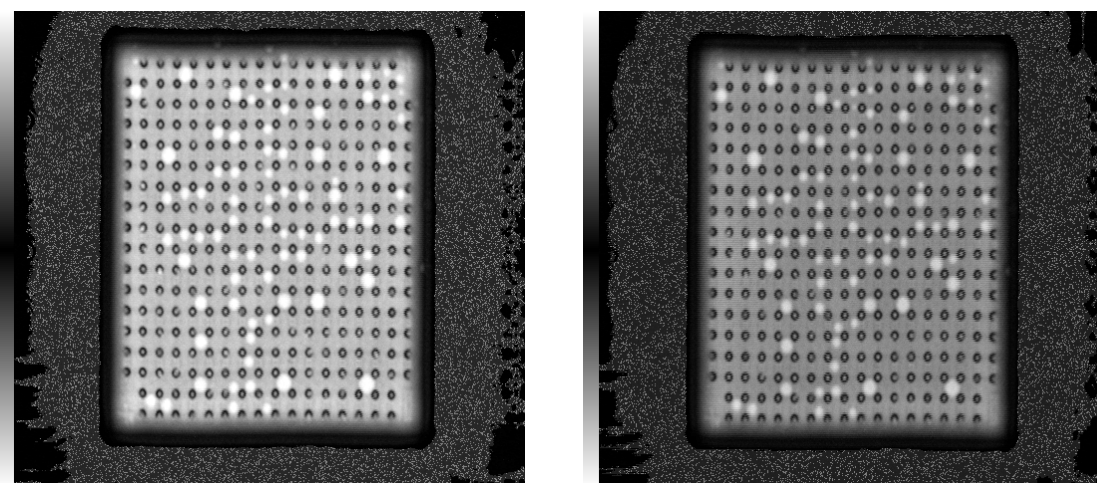


Figure 6-70 CSAM images at 0 hours (left) and 1000 hours (right);no delamination;

FA102x2 OSP TL-Underfill D, Board Number F30

6.1.3.5 FA10 4x4 HTS Results (OSP & Ni/Au : TL-Underfill C & TL-Underfill D)

The High Temperature Storage reliability data provided in this section was for the test vehicle as described in Section 4.1.1.4. A summary of the test vehicle performance is shown in the table below. The results are presented on a pass/fail basis for the High

Temperature Storage Test as described in the JEDEC specification JESD22-A103-B, condition B. The integrity of the solder interconnects was determined via electrical continuity testing at 200 cycle intervals. If the components passed the test, the result of the test would be 'Passed' and the comments would be '1000 hours' indicating the last time that the parts were evaluated. If the components failed any of the electrical continuity readouts prior to 1000 hours, the result of the test would be 'Fail' and the comments section shows at what readout the components failed. The CSAM images in figure show that there was no delamination between the die and the underfill layer as a result of the HTS accelerated life test.

Table 6-21 HTS Results for FA10 4x4 Test Vehicles

Test Die & Board	Substrate Metallization	TL - Underfill Material	Board #	# of Parts Tested	Result of HTS Test [150oC, 1000 hours]	Comments
FA10 4x4 : Test Vehicle Description in Section 4.1.1.4	Cu/Ni/Au	C	F05	8	Fail	100% failed at 800 hours
			F14	10	Fail	100% failed at 800 hours
			F15	10	Fail	100% failed at 800 hours
		D	F24	8	Fail	1 failed at 400, 7 at 800
			F26	9	Fail	100% failed at 800 hours
			F28	9	Fail	100% failed at 800 hours
	Cu/OSP	C	F14	9	Passed	1000 hours
			F16	6	Passed	1000 hours
			F17	6	Passed	1000 hours
			F18	3	Passed	1000 hours
		D	F30	9	Passed	1000 hours
			F33	9	Passed	1000 hours
			F25	7	Passed	1000 hours

All of the FA10 4x4 Ni/Au samples failed the high temperature storage life test and all of the FA10 4x4 OSP samples passed 1000 of high temperature storage life testing at 150 °C for 1000 hours.

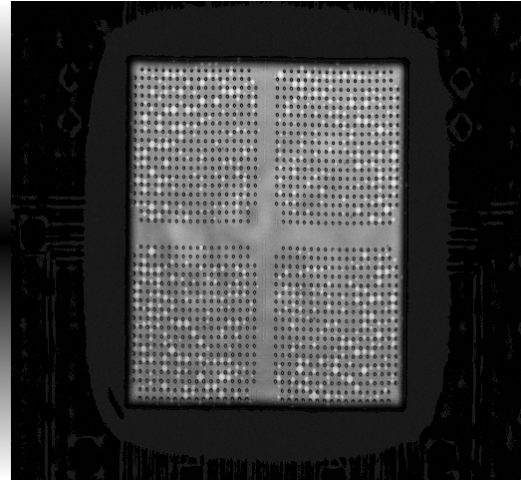
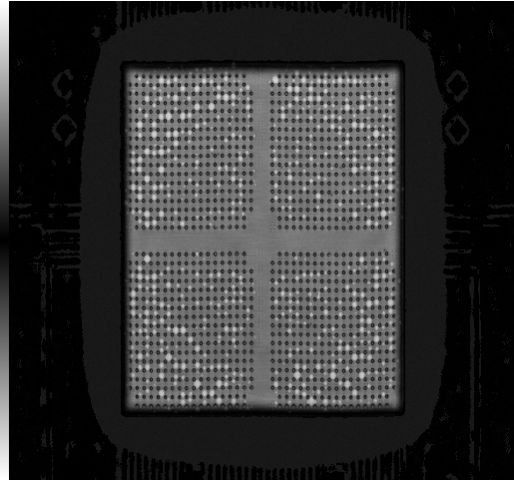


Figure 6-71 CSAM images at 0 hours (left) and 400 hours (right);no delamination;

FA104x4 Ni/Au TL-Underfill C, Board Number F15

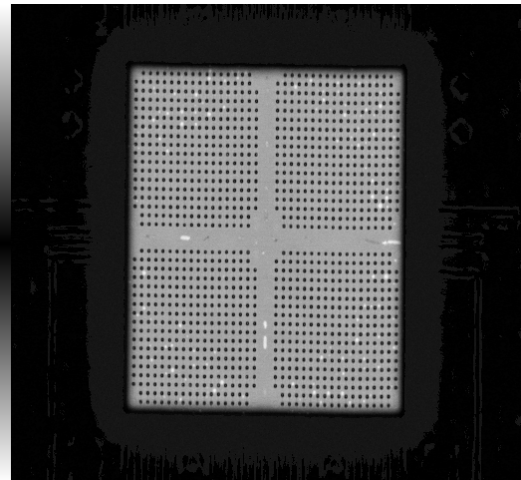
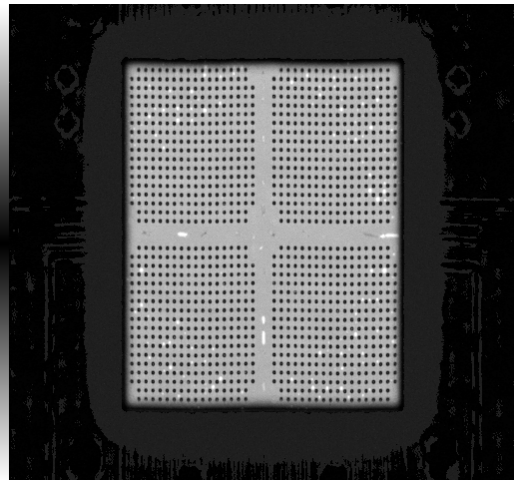


Figure 6-72 CSAM images at 0 hours (left) and 800 hours (right);no delamination;

FA104x4 Ni/Au TL-Underfill D, Board Number F28

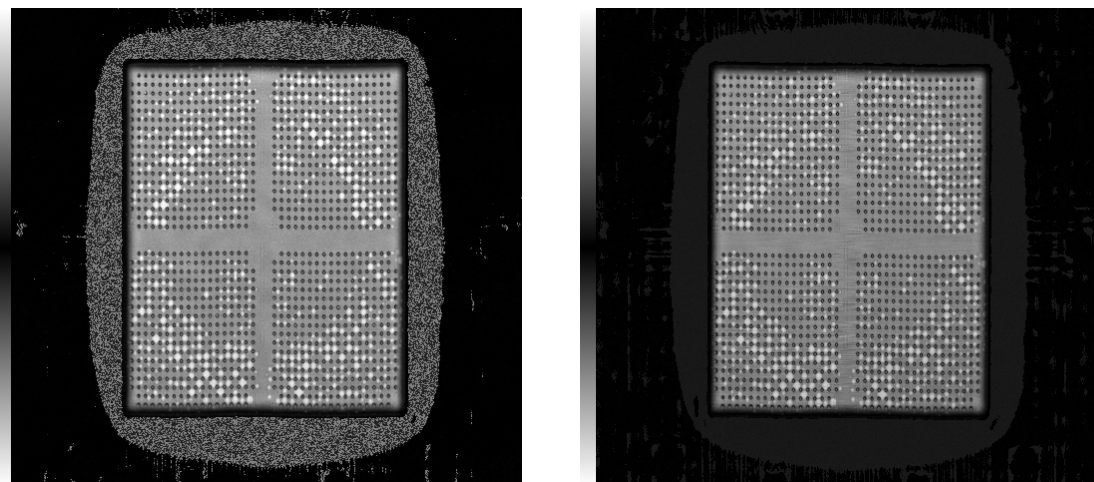


Figure 6-73 CSAM images at 0 hours (left) and 400 hours (right);no delamination;

FA104x4 OSP TL-Underfill C, Board Number F14

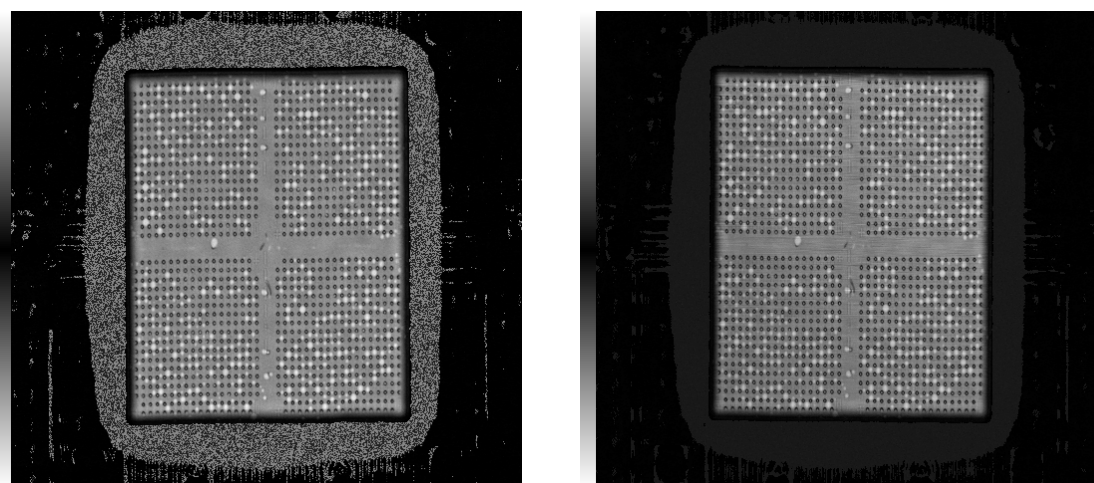


Figure 6-74 CSAM images at 0 hours (left) and 400 hours (right);no delamination;

FA104x4 OSP TL-Underfill D, Board Number F33

6.1.4 High Temperature Storage Discussion

The high temperature storage test as described in the JEDEC standard, JESD22-A103-B, is often used by component manufacturers to accelerate the growth of brittle intermetallics in the solder joint. The failures seen throughout the proceeding sections are expected to be a result of the formation of brittle Au-Sn intermetallics. The growth of

brittle intermetallic platelets within the solder joint was a result of the Au from the substrate metallurgy migrating over time throughout the solder joint where brittle, ‘weak’ regions of the solder joint were formed and these regions served as a crack initiation sites. At the high temperature storage setting of 150 °C the solder joints were stressed at a relatively low level since they were close to the stress free temperature of the assembly, which was assumed to be the reflow temperature of the solder. Although, the assemblies were at a relatively low stress state the solder joints were vulnerable at this high temperature because both underfill materials had low glass transition temperatures and at the test temperature of 150 °C the modulus of both underfills was around ~11 MPa. This means that the underfill was not providing much assistance in the way of stress distribution at this high temperature. Looking at the data as a whole: 5.94% of the components with the Cu/Ni/Au substrate metallization passed HTS, while 100% of the Cu/OSP components passed. 92.93% of the components with the Cu/Ni/Au substrate metallization failed at the 800 hours readout.

In general, the high temperature storage test can be used to accelerate many chemical and physical failure mechanisms that are accelerated with temperature. The Arrhenius equation is often used to model these mechanisms, where the reaction rate is related to temperature:

$$K = A \exp\left(\frac{-Ea}{kT}\right) \quad (6-3)$$

Where the chemical reaction speed is K , Ea is the activation energy (eV), k is Boltzmann’s constant, T is the temperature (K), and A is a constant. If there was failure data obtained at more than one temperature an estimate of the activation energy would be

made, and the acceleration factor for the intermetallic growth based failure mechanism could be determined.

6.1.5 SEM images of Failures

6.1.5.1 Fatigue Cracks

Fatigue of solder joints is believed to play a role in 90% of all mechanical and electrical failures [Tummala, 2001]. Although this statement applies to solder joints in general, flip chip solder joints typically represent the ‘worst case’ scenario in terms of solder fatigue, due to the general lack of compliance of the solder joints. Most of the assemblies that were investigated throughout this research showed fatigue cracks at the top of the joint, however there were a few assemblies with cracks along the substrate side of the bump (shown in the figure below). These cracks were a result of very small mask openings and hence the elevated stress state at the bottom of the bump caused the bump to fracture. There were a couple of solder joints that failed in the intermetallic layer, this is discussed in detail in Section 5.2.6.3.

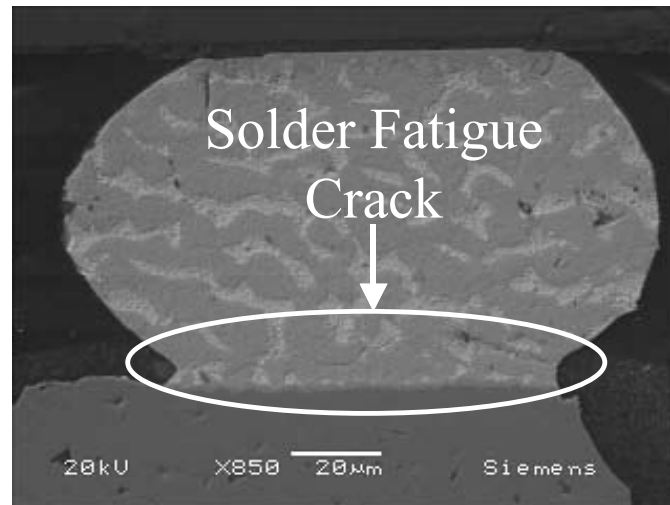


Figure 6-75 PB8 2x2 OSP: Crack at substrate side [F04 #1]

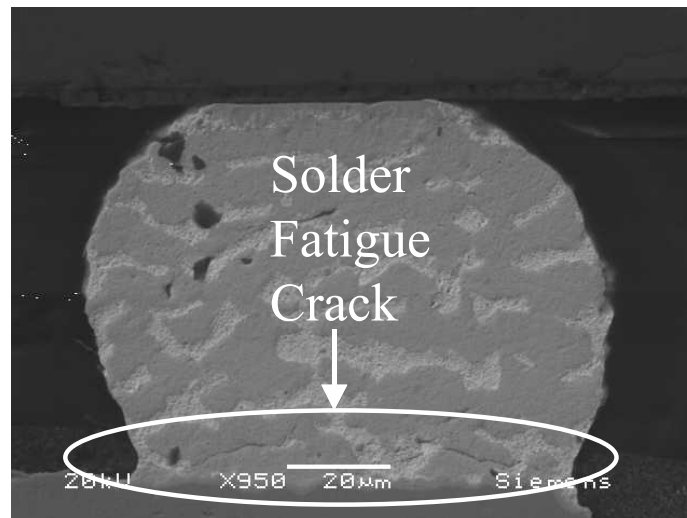


Figure 6-76 Solder Fatigue Crack Substrate Side PB8 2x2 [F04 #1]

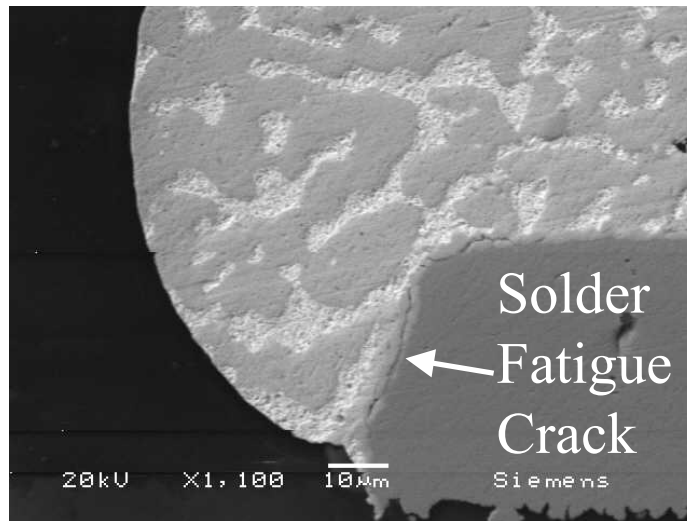


Figure 6-77 Crack at top of pad metallization [F13 #1]

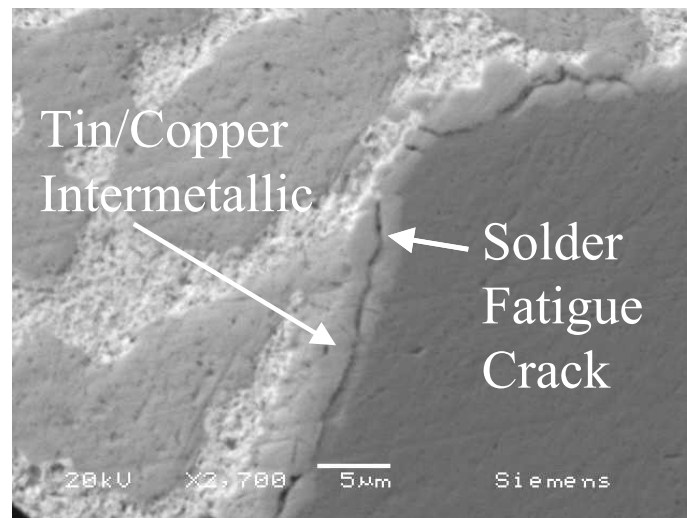


Figure 6-78 Crack at top of pad metallization [F13 #1] – Zoom

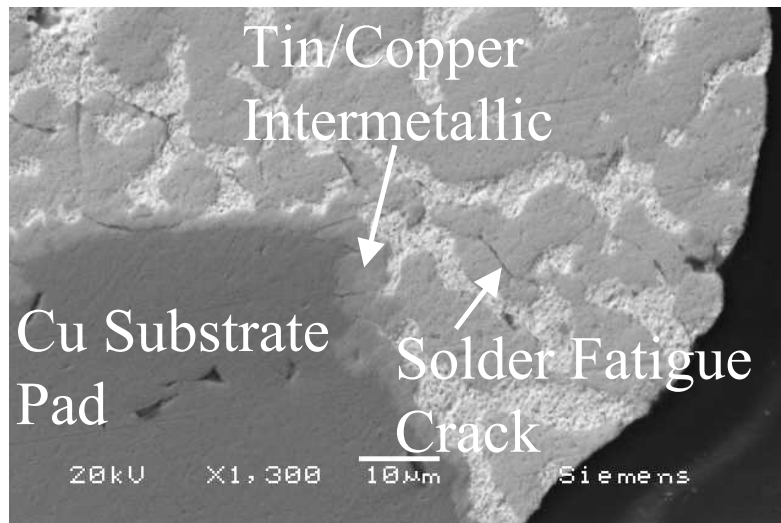


Figure 6-79 Small crack at right of solder joint [F13 # 1] – Zoom

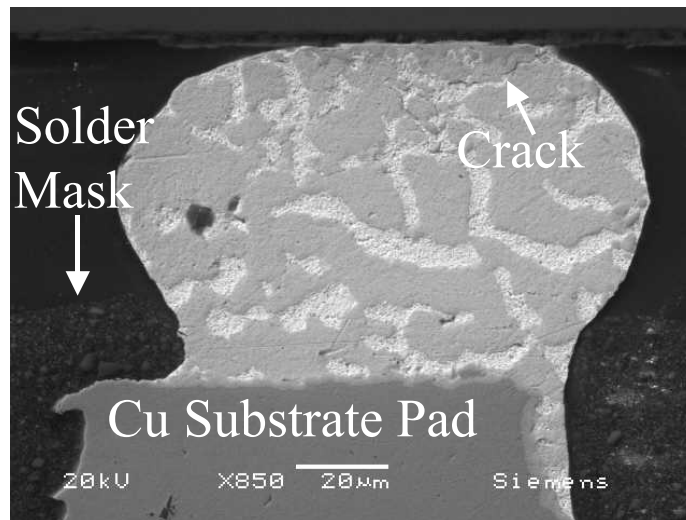


Figure 6-80 Crack at top of solder joint [F14 # 2]

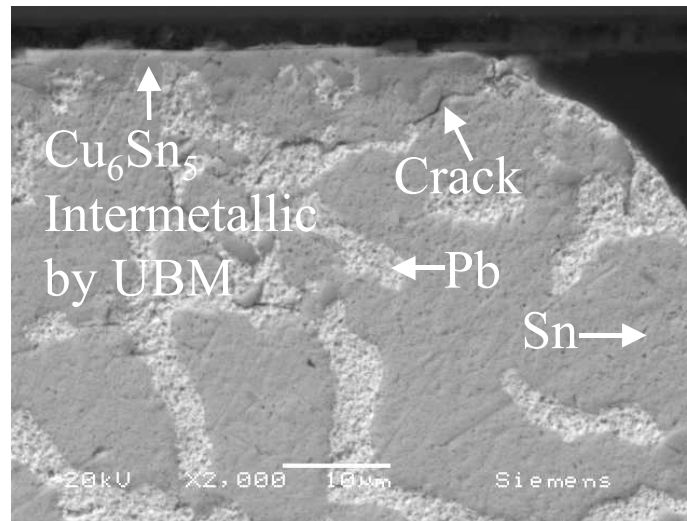


Figure 6-81 Crack at top of solder joint [F14 # 2] – Zoom

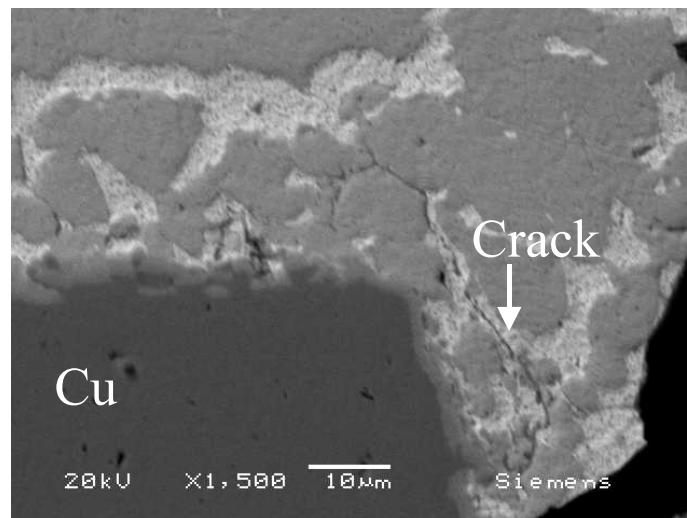


Figure 6-82 Small crack in joint [F29 #7]

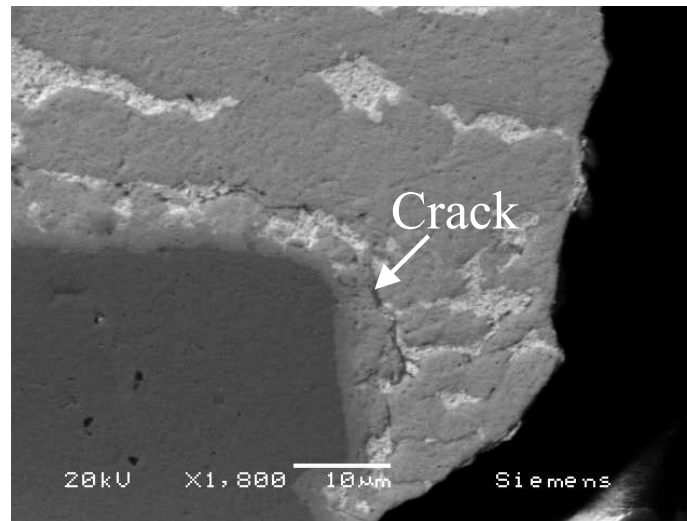


Figure 6-83 Small crack at bottom of joint [F29 #7]

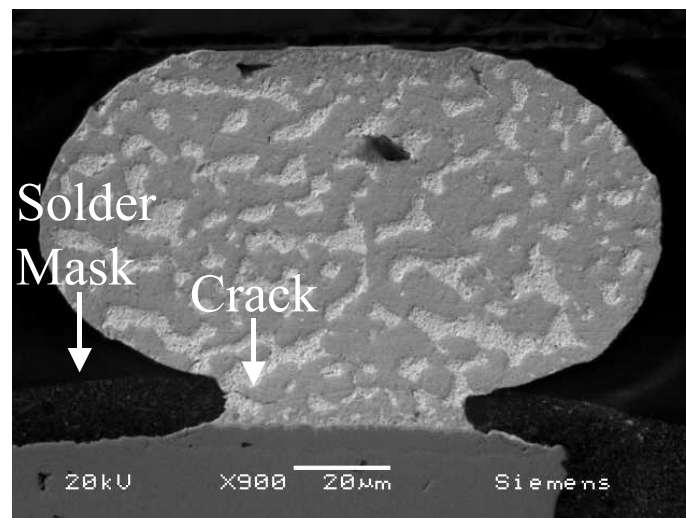


Figure 6-84 PB8 2x2 Ni/Au: Poor solder joint shape and potential crack at bottom of joint

[F10 #1]

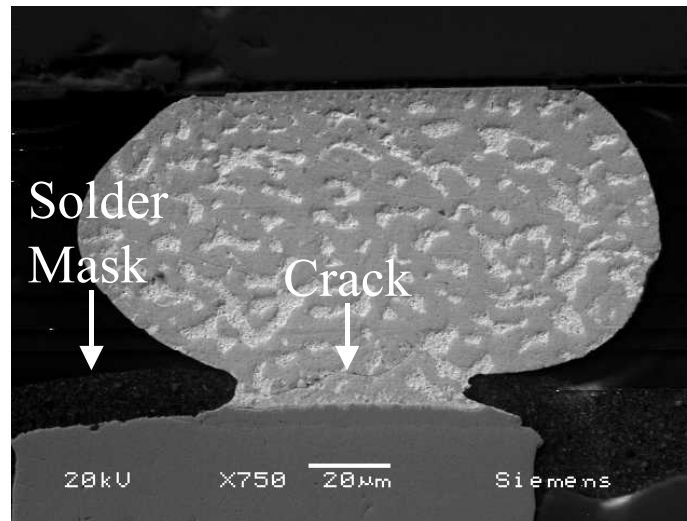


Figure 6-85 PB8 2x2 Ni/Au: Poor solder joint shape and potential crack at bottom of joint

[F10 #1]

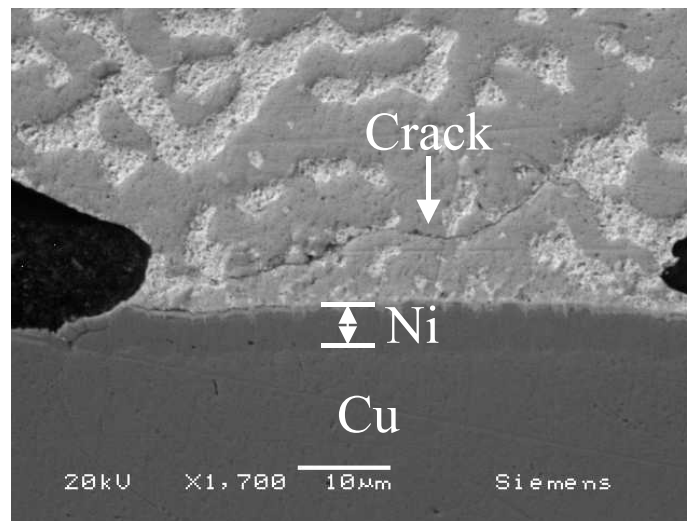


Figure 6-86 PB8 2x2 Ni/Au: Poor solder joint shape and potential crack at bottom of joint

[F10 #1]-Zoom

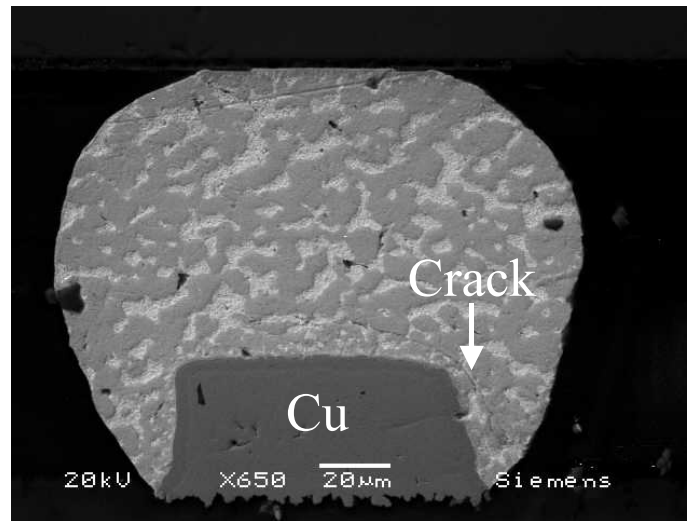


Figure 6-87 PB8 2x2 Ni/Au: Crack at substrate side of joint [F12 #2]

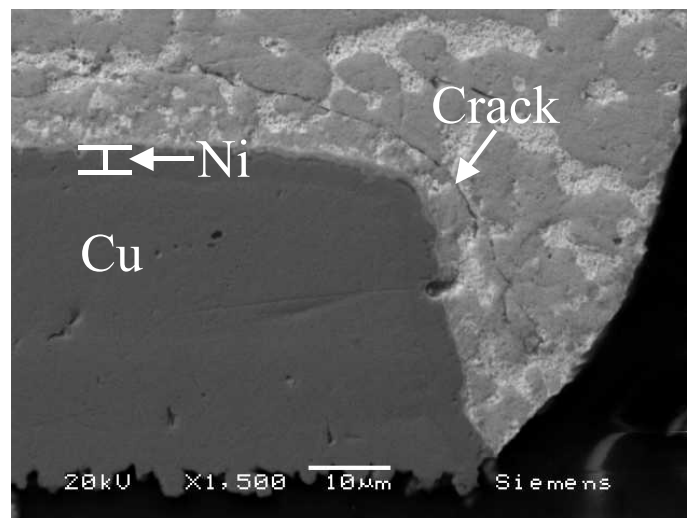


Figure 6-88 PB8 2x2 Ni/Au: Crack at substrate side of joint [F12 #2] – Zoom

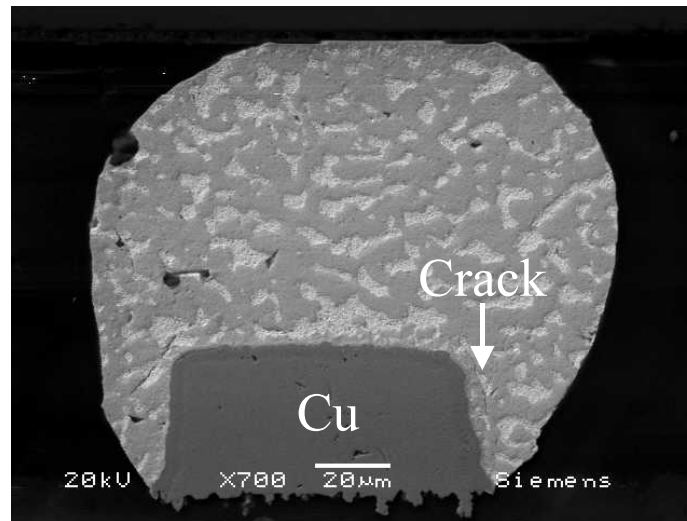


Figure 6-89 PB8 2x2 Ni/Au: Crack at substrate side of joint [F12 #2]

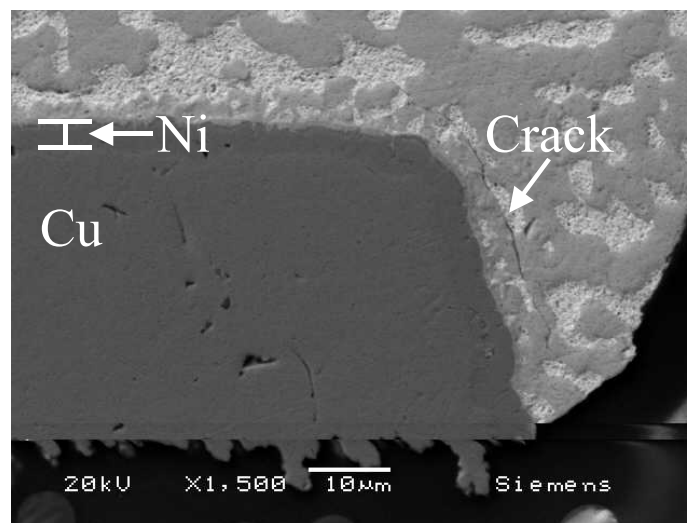


Figure 6-90 PB8 2x2 Ni/Au: Crack at substrate side of joint [F12 #2] – Zoom

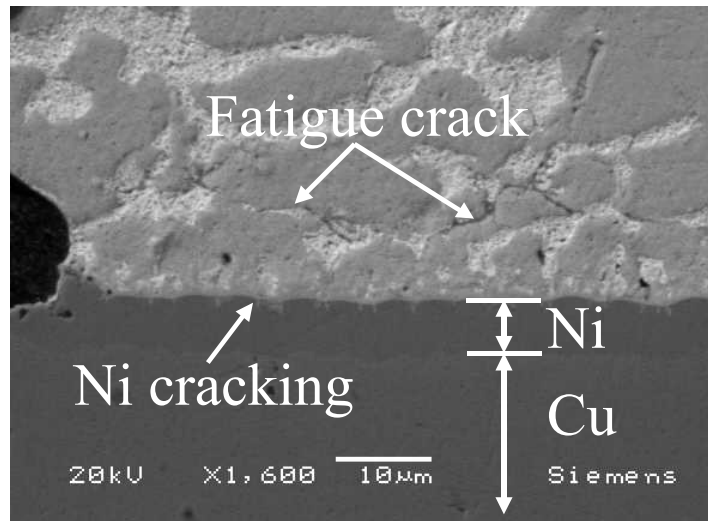
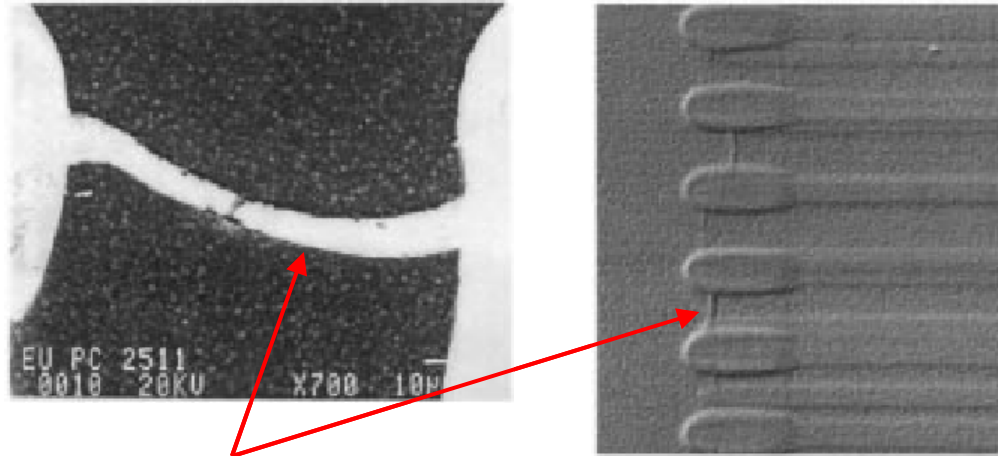


Figure 6-91 PB8 2x2 Ni/Au: Crack at the substrate side of the die [F34 #2] – Zoom

6.1.5.2 Discussion of Solder Extrusion into Underfill Voids

The focus of the modeling effort described in this thesis was fatigue cracking of solder joints, however, there was another mode of failure discovered throughout the failure analysis effort, solder extrusion. Due to the design of the test vehicles the solder extrusions were not caught via an electrical resistance shift, rather the extrusions were found when cross sectioning rows of bumps to inspect for solder fatigue cracks. Solder extrusion into underfill voids is a common problem in for flip chip assemblies and many researchers have documented the extrusions for eutectic solder as well as lead free solders [Wang, 2001; Genovese, 2001; Hou, 2001; Patwardhan, 2002]. Solder shorts can be caused by either solder extruding into an underfill micro-void or into underfill cracks. The later shorting mechanism is shown in the figure below.



Solder Extrusion into Underfill Crack

Figure 6-92 Solder Extrusion into Underfill Cracks [Hou, 2001]

The only solder extrusion mechanism that was found throughout the failure analysis conducted for this research was solder extrusion into underfill voids. Solder which is a relatively ductile material with a melting temperature of 183 °C extrudes into small voids because the no-flow underfill (which has a much higher CTE) contracts around the solder resulting in a hydrostatic stress state on the small solder joints. This hydrostatic stress state basically pushes the underfill through the small underfill voids that are adjacent to the solder bump. If an underfill void bridges the gap between two solder bumps then an electrical short will form, rendering the device useless. This is the type of shorting that was found on many of the perimeter array devices, where the pitch was small, either 150 or 203 microns.

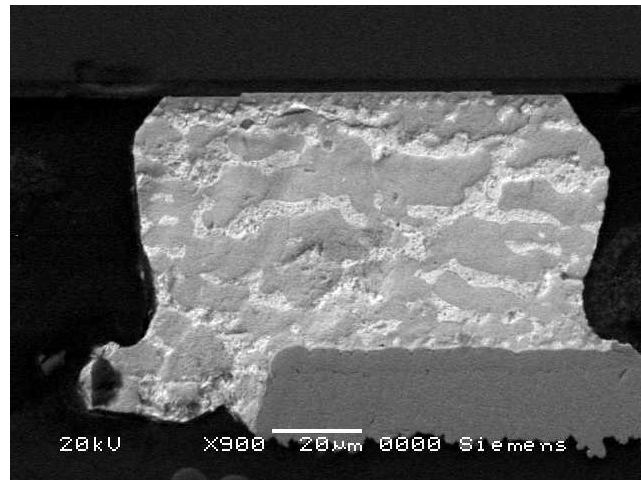


Figure 6-93 Solder Extrusion for PB6 after 300 AATC Cycles

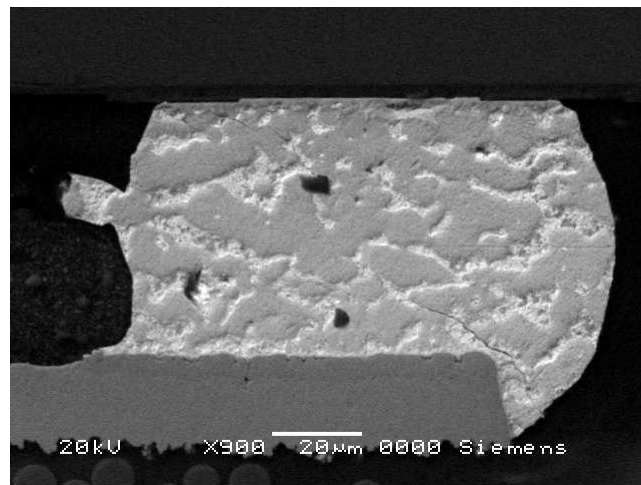


Figure 6-94 Solder Extrusion for PB6 after 300 AATC Cycles, Extrusion Over Mask

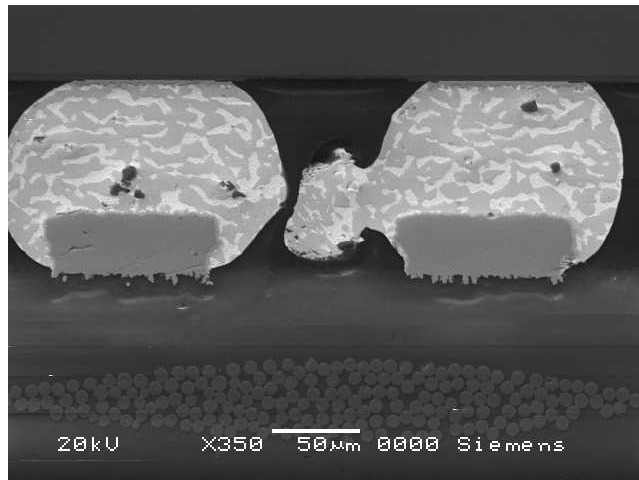


Figure 6-95 Extrusion no-short PB8 400 cycles

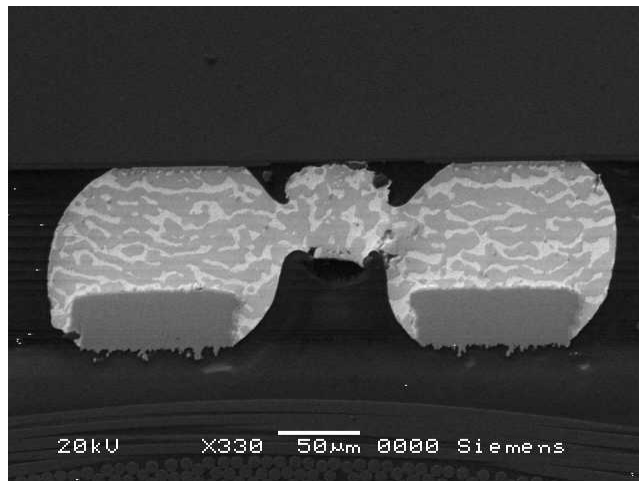


Figure 6-96 Extrusion Short PB8 400 cycles AATC

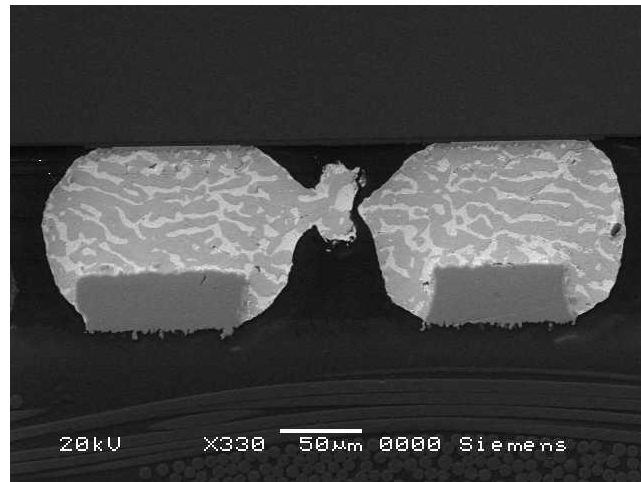


Figure 6-97 Extrusion no-short PB8 400 cycles

7 ANALYTICAL MODEL VALIDATION

This section is intended to outline the utility of the model and show the prediction capabilities of the model developed in Chapter 5 in comparison to the prediction of cycles to failure with FEM using the methods developed in Chapter 4. The components that were used for the case study were both perimeter and area array packages. These test vehicles were described in Table 7-1 below, but also in Sections 4.1.1.4, 4.1.1.6, and 4.1.1.8. For the purposes of the analytical model the material properties of the composite solder/underfill layer are assumed to be the same as a solder/underfill layer with solder joints arranged in an area array format.

7.1.1 Case Study – Validation of analytical model for a PB8 4x4 Test Vehicle

To evaluate the flip chip on board predictive failure model presented additional data was collected for different flip chip on board test vehicles. These test vehicles were assembled with new underfill materials (both capillary flow materials and no-flow underfill materials). Capillary flow underfill materials were investigated to determine if the correction function model could also predict for non-no-flow underfills. The test vehicles and underfill material properties are listed in Tables 7-1 and 7-2, respectively. Please note that the test conditions for the accelerated life testing were detailed in Table 7-1.

Table 7-1 Test Vehicles used for Validation of Model

	FA10 2x2 TV (Section 4.1.1.4)	FA10 2x2 TV (Section 4.1.1.4)	PB8 4x4 TV (Section 4.1.1.6)	PB8 4x4 TV (Section 4.1.1.8)
Board thickness	0.7874mm	0.7874mm	0.7874mm	0.7874mm
Test die	FA10 2x2	FA10 2x2	PB8 4x4	PB8 4x4
Pad Openings	Square	Square	Circular	Circular
Bond Pad Finish	Cu/Ni/Au	Cu/Ni/Au	Cu/Ni/Au	Cu/OSP
Fast Flow Snap Cure Underfill	PH-Underfill B	PH-Underfill D	BS-Underfill E	BS-Underfill E
Accelerated Life Test	AATC [-55 to 125; w/ 10 min dwells]	AATC [-55 to 125; w/ 10 min dwells]	LLTS [-55 to 125; w/ 5 min dwells]	LLTS [-55 to 125; w/ 5 min dwells]

Table 7-2 Underfill Material Properties for Underfills used in Model Validation Study

	PH-Underfill B	PH-Underfill D	BS-Underfill E
Type of Underfill	Fast Flow Snap Cure	Fast Flow Snap Cure	No-Flow Fluxing
Filler Content [%]	40	62	N/A
CTE [ppm/°C]	35-40	27	85
T _g [°C]	140	155	95
Modulus [GPa]	3.2	6.5	1

Recall, the low cycle strain based fatigue approach was given by:

$$N_f = C_{\text{metallization}}(\text{Pad finish}) \cdot C_{\text{joint shape}}(A_{\text{UBM}}, A_{\text{Pad}}) \cdot C_{T_g}(\text{Underfill}) \cdot \Delta\gamma_p^{-1.29} \quad (7-1)$$

And the modified cycles to failure approach was given by:

$$N_f = C_{\text{metallization}}(\text{Pad finish}) \cdot C_{\text{joint shape}}(A_{\text{UBM}}, A_{\text{Pad}}) \cdot C_{T_g}(\text{Underfill}) \cdot N_f' \quad (7-2)$$

The prediction in cycles to failure is shown in Table 7-3.

Table 7-3 Predictions of MTTF via FEM and Analytical/Correction Function Approach,
along with experimental MTTF for four test vehicles

Prediction of Cycles to Failure	FA10 2x2 TV (Section 4.1.1.4)	FA10 2x2 TV (Section 4.1.1.4)	PB8 4x4 TV (Section 4.1.1.6)	PB8 4x4 TV (Section 4.1.1.8)
FEM	2978	3245	1930	1930
Analytical Approach	1020	850	811	1379
Experimental MTTF	920	770	1977	2140

The analytical models predicted the MTTF well, capturing the improved reliability performance of the OSP substrate metallization over the Cu/Ni/Au metallization. Although, the improved reliability results for the OSP substrate appear to be exaggerated, this is most likely a result of the simplistic description of the substrate metallization (it was defined as a categorical variable), it is recommended that further modeling efforts capture the percentage of gold on the substrate pads as a volume fraction of gold available for embrittlement/intermetallic formation (i.e. volume of gold on substrate pad/volume of solder in solder joint). Also, although there appears to be a shift in performance between the OSP and the Ni/Au substrate metallizations that shift should be closely looked at since the difference in performance was only 163 cycles and all data was obtained via 100 cycle interval readouts. IN addition, the model predicted quite well for the capillary (fast flow snap cure) underfill materials. Notice that the FEM methodology over predicted for both of the test vehicles that used capillary flow underfill materials.

The model presented in Chapter 5 was developed by regression analysis, so the prediction of MTTF for test vehicles with a similar structure to those used in the model development will likely be quite accurate (organic boards and no-flow underfill material),

it is assumed that the model will also predict quite well for capillary flow underfills on organic substrates. However, the prediction of MTTF for test vehicles with a different general structure such as those with a ceramic substrate might not be a good predictor simply because the extrapolation behavior from the original data set might not be foreseeable, however when additional experimental data becomes available the model could be updated by re-running the regression analysis with additional data or with new input parameters. It is recommended that 10 replicates for each data point be used in the future; 30 replicates were used for most of the data points in this regression analysis; however it is believed that this was not necessary.

In general, the strain based fatigue equation with correction factors could be used as a quick and easy tool to assess the reliability performance of a flip chip on board assembly. Regression techniques were used to leverage available experimental data along with knowledge about the physics of failure to develop a predictive failure model. In addition, finite element modeling is not needed so extensive training would not be necessary to run the model. The flip chip on board model presented in this thesis incorporates the use of non-traditional predictors of performance such as the glass transition temperature of the underfill material, the metallization of the substrate bond pads and the non-dimensional quantity of UBM area to the wettable substrate bond pad area. The performance of the flip chip on board model was evaluated using a different set of test vehicles than those used to generate the model. The validation study shows that the model can predict reliability performance quite well, with a maximum deviation of 59% between the predicted and actual test results.

8 SUMMARY, CONTRIBUTIONS AND RECOMMENDATIONS

8.1 Conclusions

The experimental work in conjunction with finite element modeling led to some basic conclusions for the reliability of flip chip on board assemblies. (1) Metallization of the substrate bond pads had a significant impact on the reliability performance of flip chip on board assemblies. (2) As the glass transition temperature of the underfill material decreased the reliability of the flip chip on board component also decreased, for those materials that had a T_g less than 125°C. (3) The solder joint parameter $A_{ubm} / A_{substrate\ pad}$ was used to quantify the solder joint shape, results showed that a ratio that was slightly smaller than one provided desirable reliability results.

The presented analytical model in conjunction with correction factors provided a comprehensive predictive failure model that could be used to quickly predict the MTTF of a flip chip on board component. For non-underfilled ball grid array packages (CSPs, BGAs, PBGAs, etc.) the analytical model for the total inelastic strain will likely provide an upper bound estimate of cycles to failure, since there would be no underfill layer to distribute the thermally induced stresses. For ball grid array packages that have been underfilled the presented analytical model can be expected to serve as a lower bound estimate of reliability performance.

8.2 Contributions

In an effort to address gaps in the reliability modeling of flip chip on board literature, some fundamental contributions have been made in analytical modeling of inelastic strain in addition to the incorporation of correction factors into a strain based fatigue equation.

- ❖ A complete system for predicting the cycles to failure of a flip chip on board assembly was developed. This system incorporated the use of an analytical model to determine the plastic and creep strain experienced by a solder joint while in thermal cycle. The total inelastic strain as calculated by the analytical model was then modified by various correction factors to determine a more accurate prediction of cycles to failure. This methodology was similar to that used for the fatigue strength of metals, where the fatigue strengths were modified to account for physical differences between the actual parts in use and the parts that were used to obtain the fatigue data [Norton, 2000].
- ❖ A complete analytical model was presented for the calculation of total inelastic strain of a flip chip solder joint. This model incorporates the plastic shear strain range presented by Zhang and single power law creep [Zhang, 2003; Ju, 1994].
- ❖ The growth of intermetallics generated via different substrate bond pad metallizations was quantified and the effect of the intermetallic growth on shear strength of non-underfilled assemblies was determined.
- ❖ A 2D finite element model was developed to study the effects of various input parameters on reliability performance of a flip chip on board assembly. Finite element modeling in conjunction with experimental results and regression analysis helped to quantify the effects of glass transition temperature of the underfill material and solder joint shape on the reliability performance of a flip chip on board assembly.

8.3 Future Work

The growth of intermetallics for various UBM and substrate metallurgies should be investigated as they are important in determining the reliability performance of flip chip on board assemblies. In particular, the intermetallics should be investigated for various reflow process conditions for no-flow underfill processing. In a high volume manufacturing environment it is common for assemblies to go through reflow three times (top side, bottom side, and a repair cycle). If brittle intermetallics are formed during the reflow process solder joints will be subject to failure while in the initial stress cycles experienced in shipping and handling of the components. This is particularly undesirable from a reliability standpoint because out of box failures are unacceptable to customers, mainly because customers question (1) supplier testing methods and (2) the control that a supplier has over their manufacturing process. For references pertaining to intermetallic growth please refer to the following papers: Duan *et al.* (2003), Massalski (1987), and Harper (1997).

A method for assessing the total reliability of a component should be investigated. A total reliability metric could be used to provide a comprehensive picture of the total reliability of a component, or system. If the failures of the part are statistically independent and the structure of the component is serial in nature, meaning there are no redundant parts, the component reliability can be expressed as $R_{component} = R_{part\ 1} \cdot R_{part\ 2} \cdot R_{part\ 3}$. The reliability of the individual parts in a component are multiplied together to give the total reliability of a component. For example, the reliability of a BGA is the multiplicative total of the individual parts: the device reliability, interconnect reliability, and PWB reliability. This can be extended further to a

system level reliability (for example a circuit board used in a PDA) the reliability of the circuit board assembly is the multiplicative total of the reliabilities of the individual components, their interconnections to the circuit board, and the circuit board itself.

Another challenging problem would be to use the same methodologies presented in Chapter 5 to assess the reliability performance of other component types, for example CSPs, BGAs, or column grid arrays. In addition, the current flip chip on board model could be extended as further reliability information became available.

All of the models presented in this thesis are for the prediction of cycles to failure due to low cycle fatigue; these models are specifically looking at the mean time to failure and not the rate at which failure occurs. To capture a rate effect several sets of data would need to be generated with various shape and scale parameters for the Weibull distribution, the shape could then be used as a predictor of reliability performance. The same regression techniques that are described in Appendix B could be used to fit a shape parameter as a predictor of performance. It is recommended that the future test vehicles used for reliability modeling only have 10 replicates as opposed to the 30 replicate samples that were used for most of the data analysis in this thesis. In addition, the thickness of the gold on the bond pad metallization should be altered such that the volume of gold on the bond pads could be used as a predictor as opposed to the dummy variable, metallization, which was either a 1 or a 0 for the modeling work presented in Section 5.2.5.

The “pillowing” phenomenon should be investigated in terms of reliability performance. Pillowing is when the solder joint forms a short barrel shape where the top of the barrel is attached at the UBM and there is a small ring of solder that is pushed

against the die passivation. This is believed to cause a high stress concentration in the solder where it is attached to the UBM; this is almost a pre-notched solder joint in terms of fatigue. Figure 8-1 shows and SEM image of a joint that pillowed. Notice the circular UBM and the solder that is around the UBM (there is a grain structure that is obvious in the solder ring around the UBM).

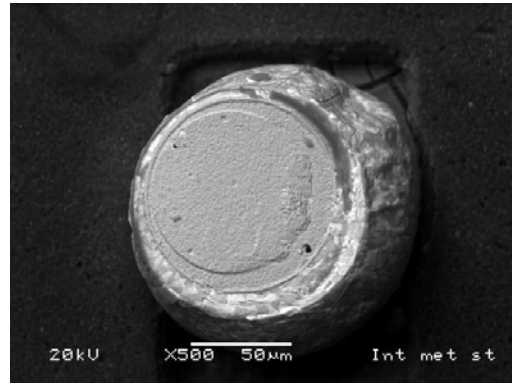


Figure 8-1 Image of Solder Joint with “Pillowing”

In addition, the effects of delamination on reliability performance should be investigated. Once the underfill delaminates from the passivation layer on the silicon die the rate of flip chip interconnect failure typically increases. The effect of delamination should be investigated in terms of reliability modeling.

A. APPENDIX – FINITE ELEMENT APDL CODE

```
! 2D APDL Code with Creep for FA102x2
! _____ !
! Jennifer Muncy !
! 2D model of a FA10 2x2 Flip Chip with underfill !
! Using Flip Chip Technologies data !
! Last Updated on October 26th - final for thesis !
! _____ !

! units are in mm, MPa
! Enter the preprocessor

FINISH
/CLEAR,NOSTART
/prep7

! _____ element types
incc = 1e-12 ! tiny increment for selecting
objects
! define element types

ET,1,plane2
KEYOPT,1,3,2
KEYOPT,1,5,0
KEYOPT,1,6,0
ET,2,plane82
KEYOPT,2,3,2
KEYOPT,2,5,0
KEYOPT,2,6,0
ET,3,plane183 ! 2D-eight node element (plane
strain on)
KEYOPT,3,3,2
KEYOPT,3,6,0
```

```

KEYOPT,3,10,0
ET,4,VISCO108                !2D-element    w/    rate    dep.
prop.(plane strain on)
KEYOPT,4,3,0
KEYOPT,4,5,0
KEYOPT,4,6,0
KEYOPT,4,7,0

ET,5,PLANE42
KEYOPT,1,1,0
KEYOPT,1,2,0
KEYOPT,1,3,2                !Plane strain on
KEYOPT,1,5,0
KEYOPT,1,6,0

!variables for changing model parameters
ele_type = 1                !which element type to use for
mesh
ln_set = 1                  !set line size manually
lsize_1 = 5
lsize_2 = 10

!_____material
properties
!define material properties
silicon=1
fr4=2
solder=3
underfill=4

!define material property:SILICON
!MP,EX,1,131E3                !silicon young's modulus
!MP,PRXY,1,0.3                !silicon poisson's ratio
!MP,ALPX,1,2.8e-6            !silicon CTE

!define material property:    FR4

```

```

!MP,EX,2,22E3                !fr4 young's modulus
!MP,PRXY,2,0.28              !fr4 poisson's ratio
!MP,ALPX,2,18e-6             !fr4 CTE

!define material property:    No flow Underfill
!MP,EX,4,2.7E3                !No Flow Underfill young's modulus
!MP,PRXY,4,0.3                !Underfill poisson's ratio
!MP,ALPX,4,75e-6              !No flow Underfill CTE
!MP,EX,4,7E3                  !Cap. Flow Underfill young's
modulus
!MP,ALPX,4,33e-6              !Cap. flow Underfill CTE

!define material property:    solder-linear elastic
!MPTEMP,1,200,450
!mpdata,ex,3,1,45500,7580
!mptemp                        !solder Elastic Modulus
!MP,PRXY,3,0.35                !Solder poisson's ratio
!MP,ALPX,3,21e-6                !Solder CTE

!_____creep
!Creep code for anands model
!TB,ANAND,3
!TBDATA,1,12.41,9400,4e6,1.5,.303,1379
!TBDATA,7,13.79,.07,1.3

!creep code for double power law
!TB,CREEP,3,1,1,1
!TBDATA,1,.40,2,5400,21,7,9500

!_____kinematic
hardening
!define material property:    SOLDER - kinematic hardening
!kinematic hardening and various E values at different temps
!From: Time-dependent material modeling for finite element
analysis of flip chips

```

```

!MPTEMP,1,280,320
!MPDATA,EX,3,1,30e3,27.14e3
!MPDATA,PRXY,3,1,.31,.31

!TB,KINH,3,2,3
!TBTEMP,280
!TBPT,,7.0e-4,21
!TBPT,,3.0e-3,41
!TBPT,,1,600
!TBTEMP,320
!TBPT,,3.0e-3,31
!TBPT,,1,200
!MP,ALPX,3,23.3e-6

!_____final      material
properties
! FR4

MPTEMP
MPTEMP,1,303,368,383,398,423,543

MPDATA,EX,2,1,22400,20680,19970,19300,17920,16000
MPDATA,EZ,2,1,22400,20680,19970,19300,17920,16000
MPDATA,EY,2,1,1600,1200,1100,1000,600,450

! FR4 Poisson's Ratio
MPDATA,NUXZ,2,1,0.1360,0.1360,0.1360,0.1360,0.1360,0.1360
MPDATA,NUXY,2,1,0.1425,0.1425,0.1425,0.1425,0.1425,0.1425
MPDATA,NUYZ,2,1,0.1425,0.1425,0.1425,0.1425,0.1425,0.1425

! FR4 Coefficient of Thermal Expansion
MPDATA,ALPX,2,1,20e-6,20e-6,20e-6,20e-6,20e-6,20e-6
MPDATA,ALPZ,2,1,20e-6,20e-6,20e-6,20e-6,20e-6,20e-6
MPDATA,ALPY,2,1,86.5e-6,86.5e-6,243e-6,400.e-6,400.e-
6,400.e-6

```

```

! FR4 SHEAR MODULUS
MPDATA, GXZ, 2, 1, 630, 600, 550, 500, 450, 441
MPDATA, GXY, 2, 1, 199, 189, 173, 157, 142, 139.3
MPDATA, GYZ, 2, 1, 199, 189, 173, 157, 142, 139.3

! Solder

MP, ALPX, 3, 21.0E-6 ! Coefficient of thermal expansion
(mm/mm C)

MPTEMP ! Clear material temperature table

MPTEMP, 1, 248, 298, 358, 398 ! Create temperature table
(Kelvin)
MPDATA, EX, 3, 1, 27390, 19650, 15270, 11680 ! Set Young's
Modulus (N/mm^2)
MPDATA, EY, 3, 1, 27390, 19650, 15270, 11680
MPDATA, EZ, 3, 1, 27390, 19650, 15270, 11680

MPDATA, GXY, 3, 1, 9782, 7018, 5454, 4171 ! G = E/(2*(1+NU))
MPDATA, GYZ, 3, 1, 9782, 7018, 5454, 4171
MPDATA, GXZ, 3, 1, 9782, 7018, 5454, 4171

MP, NUXY, 3, 0.4 ! Poisson's ratio
MP, NUYZ, 3, 0.4
MP, NUXZ, 3, 0.4

TB, MKIN, 3, 4 ! Create table for Multilinear
Kinematic Hardening (MKIN) model
TBTEMP, , STRAIN

! stress/strain values. Strain (mm/mm), stress (N/mm^2)

TBDATA, 1, 0.0010, 0.0020, 0.0030, 0.0040, 0.0050
TBTEMP, 248
TBDATA, 1, 27.39, 41.36, 47.93, 50.30, 50.77

```



```

TBTEMP, 298
TBDATA, 1, 19.65, 29.68, 34.12, 36.35, 37.24
TBTEMP, 358
TBDATA, 1, 15.27, 22.51, 26.00, 27.83, 28.64
TBTEMP, 398
TBDATA, 1, 11.68, 16.12, 18.56, 19.88, 20.55

!Single power law creep - constants by Ju
TB, CREEP, 3, 1, 1
TBDATA, 7, 1.84E-4, 5.2, 0, 6013.95, 0, 1

! Silicon

UIMP, 1, ALPX, ALPY, ALPZ, 2.6E-6, 2.6E-6, 2.6E-6
UIMP, 1, EX, EY, EZ, 1.6E5, 1.6E5, 1.6E5
UIMP, 1, GXZ, GXY, GYZ, 6.5E4, 6.5E4, 6.5E4
UIMP, 1, NUXZ, NUXY, NUYZ, 0.23, 0.23, 0.23

! Underfill (149-5 with a glass transition temperature of 62
- 335K)

!The values used for this section are an average of the
vendor supplied

!information and the values obtained via our own
measurements using DMA

!as well as TMA techniques. The reason that an average was
used is

!because the vendor has a vested interest in supplying a
lower CTE, and

!higher Tg material and since for example the Tg is a
actually a range

!of temperatures the vendor might have simply used the
beginning of the

!Tg range, but for the purposes of FEM we define Tg as the
center and

!define the range -10 and +10 degrees to either side of the
actual Tg value.

MPTEMP

```

```

MPTEMP,1,248,325,345,398
MPDATA,EX,4,1,2.2E3,2.2E3,15,15
MPDATA,EY,4,1,2.2E3,2.2E3,15,15
MPDATA,EZ,4,1,2.2E3,2.2E3,15,15

MPDATA,ALPX,4,1,83.6E-6,83.6E-6,198.5E-6,198.5E-6
MPDATA,ALPY,4,1,83.6E-6,83.6E-6,198.5E-6,198.5E-6
MPDATA,ALPZ,4,1,83.6E-6,83.6E-6,198.5E-6,198.5E-6

MPDATA,NUXZ,4,1,0.30,0.30,0.30,0.3
MPDATA,NUXY,4,1,0.30,0.30,0.30,0.3
MPDATA,NUYZ,4,1,0.30,0.30,0.30,0.3

MPDATA,GXZ,4,1,.846E3,0.846E3,5.77,5.77
MPDATA,GXY,4,1,.846E3,0.846E3,5.77,5.77
MPDATA,GYZ,4,1,.846E3,0.846E3,5.77,5.77

!UIMP,4,EX,EY,EZ,2.4E3,2.4E3,2.4E3 !No Flow Underfill
young's modulus
!UIMP,4,GXZ,GXY,GYZ,.923E3,.923E3,.923E3
!UIMP,4,NUXZ,NUXY,NUYZ,0.3,0.3,0.3 !Underfill poisson's
ratio (no flow & cap.flow)
!UIMP,UF,ALPX,4,75e-6 !No flow Underfill CTE
!UIMP,UF,EX,4,7E3 !Cap Flow Underfill young's
modulus

!_____general
dimensions
!Dimensions of FA102x2
bump_r = .06 !bump diameter of 120 microns
ubm_r = .051 !UBM diameter of 102 microns
pad_r = .051
pitch = .127 !pitch
fc_thk = .600 !flip chip thickness
fr4_thk = .7874 !fr4 board thickness, as measured
stnd_off = .095 !stand off btwn die and FR4 board
die = 2.54 !die size, 2x2inches

```

```

fillet= .8*fc_thk+stnd_off      !fill fillet rad. - approx.
it with arc.

mask = .010                      !soldermask thickness

bump_x = .076                    !first bump x location
bump_y = 2.346                  !all bumps y location
bump_z = -0.5*stnd_off          !all bumps z location

!_____fr4
K,1,0,0,0
K,2,0,fr4_thk,0
K,3,2*die,fr4_thk,0
K,4,2*die,0,0
A,1,2,3,4

!_____die

K,5,0,fr4_thk+stnd_off,0
k,6,0,fr4_thk+stnd_off+fc_thk,0
k,7,die,fr4_thk+stnd_off+fc_thk,0
k,8,die,fr4_thk+stnd_off,0
A,5,6,7,8

!_____bump 1 (closest to
the DNP)

K,9,0.5*pitch-ubm_r,fr4_thk+stnd_off,0
K,10,0.5*pitch-pad_r,fr4_thk+mask,0
k,11,0.5*pitch+ubm_r,fr4_thk+stnd_off,0
K,12,0.5*pitch+pad_r,fr4_thk+mask,0
K,13,0.5*pitch+bump_r,fr4_thk+.5*stnd_off+mask,0
K,14,0.5*pitch-bump_r,fr4_thk+.5*stnd_off+mask,0
K,15,0.5*pitch-pad_r,fr4_thk,0
K,16,0.5*pitch+pad_r,fr4_thk,0
larc,9,10,14
larc,11,12,13
l,10,15

```

```

l,12,16
l,9,11
l,15,16

l sel,all
Al,9,12,10,11,13,14
!_____generating the remainder
of the bumps
asel,s,area,,3
AGEN,9,all,,.254,0,0,,0
asel,all
aplot
!_____solder mask
K,65,0,fr4_thk+mask,0
K,66,2*die,fr4_thk+mask,0
A,2,65,66,3
APTN,3,4,5,6,7,8,9,10,11,12    !Partition areas, then will
add back together.
AADD,13,14
AADD,17,18
AADD,20,21
AADD,23,24
AADD,26,27
AADD,29,30
AADD,32,33
AADD,35,36
AADD,38,39

!_____RE NUMBERING

NUMCMP,kp
NUMCMP,line
NUMCMP,area
!_____

```

! _____underfill

K,67,die,fr4_thk+mask,0

A,65,5,8,67

APTN,3,22

AADD,23,26

APTN,4,25

AADD,23,26

APTN,5,27

AADD,25,26

APTN,6,28

AADD,27,26

APTN,7,29

AADD,27,28

APTN,8,30

AADD,28,29

APTN,9,31

AADD,29,30

APTN,10,32

AADD,30,31

APTN,11,33

AADD,31,32

NUMCMP,kp

NUMCMP,line

NUMCMP,area

! _____

k,68,die+fillet,fr4_thk+mask,0

k,69,die,fr4_thk+stnd_off+.7*fc_thk,0

k,70,die+.5*fillet,fr4_thk+stnd_off+.1*fillet,0

larc,69,68,70

l,67,68

l,67,69

AL,100,99,98

AADD,31,32

```
AADD,1,12,13,14,15,16,17,18,19,20,21
```

```
!_____overlap
```

```
asel,all
```

```
aglu,e,all
```

```
NUMCMP,kp
```

```
NUMCMP,line
```

```
NUMCMP,area
```

```
!_____setting
```

```
line sizes
```

```
lsel,s,line,,7 !RHS & LHS of solder bumps
```

```
lsel,a,line,,8
```

```
lsel,a,line,,13
```

```
lsel,a,line,,17
```

```
lsel,a,line,,19
```

```
lsel,a,line,,23
```

```
lsel,a,line,,25
```

```
lsel,a,line,,29
```

```
lsel,a,line,,31
```

```
lsel,a,line,,35
```

```
lsel,a,line,,37
```

```
lsel,a,line,,41
```

```
lsel,a,line,,43
```

```
lsel,a,line,,47
```

```
lsel,a,line,,49
```

```
lsel,a,line,,53
```

```
lsel,a,line,,55
```

```
lsel,a,line,,59
```

```
LESIZE,all,,7,,,,1
```

```

lsel,s,line,,9          !RHS & LHS of bottom of solder
bumps
lsel,a,line,,10
lsel,a,line,,14
lsel,a,line,,16
lsel,a,line,,20
lsel,a,line,,22
lsel,a,line,,26
lsel,a,line,,28
lsel,a,line,,32
lsel,a,line,,34
lsel,a,line,,38
lsel,a,line,,40
lsel,a,line,,44
lsel,a,line,,46
lsel,a,line,,50
lsel,a,line,,52
lsel,a,line,,56
lsel,a,line,,58
LESIZE,all,, ,2, , , , ,1

lsel,s,line,,11         !UBM of bump
lsel,a,line,,18
lsel,a,line,,24
lsel,a,line,,30
lsel,a,line,,36
lsel,a,line,,42
lsel,a,line,,48
lsel,a,line,,54
lsel,a,line,,60
LESIZE,all,, ,6, , , , ,1

lsel,s,line,,12         !bot of bump
lsel,a,line,,15
lsel,a,line,,21
lsel,a,line,,27

```

```
l sel,a,line,,33
```

```
l sel,a,line,,39
```

```
l sel,a,line,,45
```

```
l sel,a,line,,51
```

```
l sel,a,line,,57
```

```
LESIZE,all,,6,,1
```

```
l sel,s,line,,74
```

```
!bot of die
```

```
l sel,a,line,,75
```

```
l sel,a,line,,77
```

```
l sel,a,line,,78
```

```
l sel,a,line,,79
```

```
l sel,a,line,,80
```

```
l sel,a,line,,81
```

```
l sel,a,line,,82
```

```
LESIZE,all,,6,,1
```

```
l sel,s,line,,65
```

```
!top of solder mask
```

```
l sel,a,line,,66
```

```
l sel,a,line,,67
```

```
l sel,a,line,,68
```

```
l sel,a,line,,69
```

```
l sel,a,line,,70
```

```
l sel,a,line,,71
```

```
l sel,a,line,,72
```

```
LESIZE,all,,10,,1
```

```
!_____
```

```
asel,s,area,,2,10
```

```
aatt,3,,2
```



```
amesh,all
```

```
asel,s,area,,12,21
```

```
aatt,4,,1
```

```
amesh,all
```

```
asel,s,area,,11
```

```
aatt,2,,1
```

```
amesh,all
```

```
asel,s,area,,1
```

```
aatt,1,,1
```

```
amesh,all
```

```
asel,all
```

```
!_____entering solution
```

```
/solu
```

```
!_____boundary
```

```
conditions
```

```
NSEL,s,loc,x,-incc,incc !select the center axis
```

```
D,all,UX,0
```

```
nsel,s,loc,x,-incc,incc
```

```
nsel,r,loc,y,-incc,incc
```

```
D,all,uy,0
```

```
LSEL,all
```

```
!_____load steps
```

```
nlgeom,on !turn on large deformation
```

```
autots,on ! turn on automatic time stepping  
for solution
```

```
!antype,0 !Static solution
```

```
TREF,456      !set reference temperature at stress free
temp-cure temp for underfill (no flow = 183)
```

```
!Begin applying load steps
```

```
!First load step
```

```
allsel,all
```

```
BF,all,temp,298      !apply temperature-298...room temp
```

```
TIME,150             !set time at end of load step
```

```
NSUBST,3,9999,1      !set substep divisions
```

```
OUTRES,all,last      !output only last substep result, this
is important - file will be enormous otherwise
```

```
SOLVE
```

```
allsel,all
```

```
BF,all,temp,298
```

```
TIME,750
```

```
NSUBST,3,9999,1
```

```
OUTRES,all,last
```

```
SOLVE
```

```
allsel,all
```

```
BF,all,temp,398
```

```
TIME,810
```

```
NSUBST,5,9999,1
```

```
OUTRES,all,last
```

```
SOLVE
```

```
allsel,all
```

```
BF,all,temp,398
```

```
TIME,1410
```

```
NSUBST,5,9999,1
```

```
OUTRES,all,last  
SOLVE
```

```
allsel,all  
BF,all,temp,218  
TIME,1470  
NSUBST,5,9999,1  
OUTRES,all,last  
SOLVE
```

```
allsel,all  
BF,all,temp,218  
TIME,2070  
NSUBST,5,9999,1  
OUTRES,all,last  
SOLVE
```

```
allsel,all  
BF,all,temp,398  
TIME,2130  
NSUBST,5,9999,1  
OUTRES,all,last  
SOLVE
```

```
allsel,all  
BF,all,temp,398  
TIME,2730  
NSUBST,5,9999,1  
OUTRES,all,last  
SOLVE
```

```
allsel,all  
BF,all,temp,218  
TIME,2790  
NSUBST,5,9999,1  
OUTRES,all,last  
SOLVE
```

```
allsel,all  
BF,all,temp,218  
TIME,3390  
NSUBST,5,9999,1  
OUTRES,all,last  
SOLVE
```

```
allsel,all  
BF,all,temp,398  
TIME,3450  
NSUBST,5,9999,1  
OUTRES,all,last  
SOLVE
```

```
allsel,all  
BF,all,temp,398  
TIME,4050  
NSUBST,5,9999,1  
OUTRES,all,last  
SOLVE
```

```
allsel,all  
BF,all,temp,218  
TIME,4110  
NSUBST,5,9999,1  
OUTRES,all,last
```

SOLVE

allsel,all

BF,all,temp,218

TIME,4710

NSUBST,5,9999,1

OUTRES,all,last

SOLVE

allsel,all

BF,all,temp,398

TIME,4770

NSUBST,5,9999,1

OUTRES,all,last

SOLVE

B. APPENDIX - STEP BY STEP REGRESSION ANALYSIS TO CALCULATE CORRECTION FACTORS

When determining appropriate correction factors, or correction functions, for any component it is advisable to review all possible parameters that might influence reliability performance of a given component. One way to visualize all of the various factors and how they are interrelated is with a ‘fishbone’ diagram, the figure below shows a diagram of all the factors that influence reliability performance of flip chip on board assemblies.

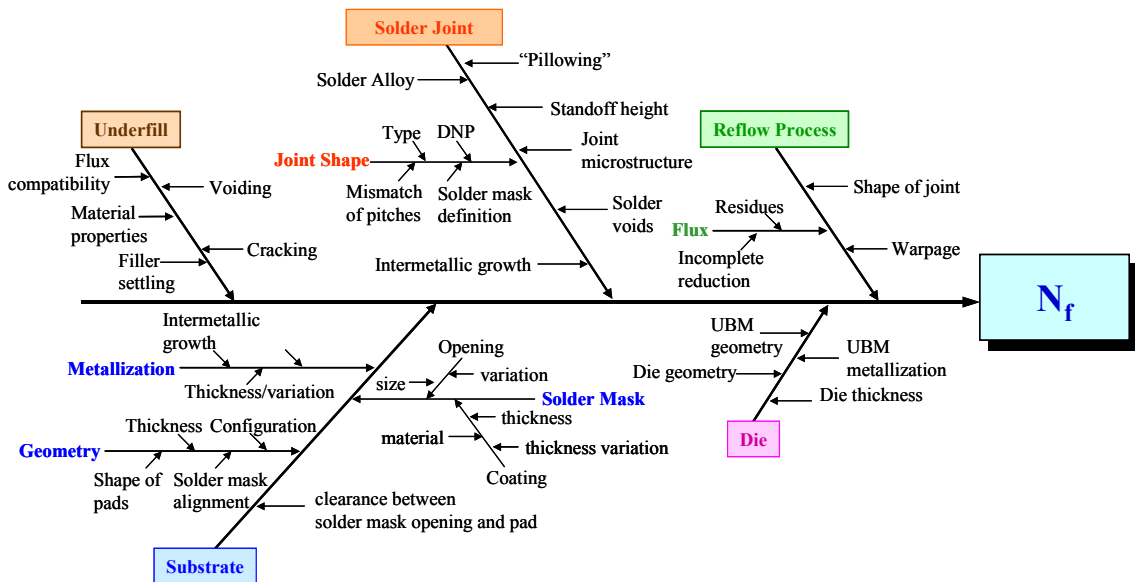


Figure B-1 Fishbone Diagram of Potential Predictors of Reliability Performance

The diagram above is obviously too dense to isolate given predictors in a timely/realistic fashion, therefore the number of correction factors actually studied was narrowed to those factors detailed in the following table.

Table B-1 Correction Factors Studied in Regression Analysis

Correction Factors Studied	Column in Table 2	Why it was chosen
Location flip chip on the board (site # on the circuit board)	C	This should not show up as a predictor if the parts experience the same out of plane deformation while in thermal cycle/shock.
Substrate bond pad metallization	D	Gold embrittlement in flip chip interconnects is a well documented reliability concern.
% Area of voiding in the underfill layer	F	Voiding in the underfill layer causes extrusion failures between interconnects; often in advance of when an underfill crack followed by a hairline extrusion would occur.
Frequency of cycles per hour	G	LLTS testing uses a shorter dwell time in the hot chamber, therefore there would be less creep damage and hence a longer life of the component/interconnects
Solder joint configuration (Perimeter vs. area)	H	For the same size die, area array devices have more bumps and therefore more opportunities for failure
Size of the die	I	The larger the die the larger the distance from neutral point to the outermost bumps.
Number of I/O	J	The greater the I/O count the more opportunities for failure.
Average pad opening	K	Small mask openings or poor mask misregistration could result in solder joints that have stress concentrations at the substrate side of the solder joint
UBM diameter	L	Needed this to calculate the next parameter
Area ratio [UBM area/Pad area]	M	This is a non-dimensional metric relates the size of the bump to the mask openings size
CTE of underfill	N	The higher the CTE of the underfill the greater the mismatch between the silicon and the underfill layer, this increases the stresses/strains on the solder joints while in thermal cycle.

Once the experimental data was obtained, it was arranged into a spreadsheet with each potential predictor detailed in a column format as shown in the table below.

Table B-2 Raw Data for Regression Analysis

Test Vehicle	Board #	Site	Metalization (categorical input) X=0 for Ni/Au; X=1 for OSP	Failed at (# of cycles)	% area voiding	Frequency of Cycles per Hour (2.72cph AATC -55 to 125; 2.30cph AATC -40 to 125; 6cph LLTS)	P/A (Categorical Variable) X=0 for P; X=1 for A	Die Size (Categorical Variable) X=0 for 5mm; X=1 for 10mm	Number of I/O	Average Pad Opening (mm*mm)	UBM Diameter (mm)	UBM area over Average pad Area	CTE of Underfill (ppm/°C)	Tg of underfill (°C)	Modulus of Underfill (Gpa)	Board Thickness (mm)	Total Strain from Analytical Model (%)	Predicted Cycles to Failure with Analytical Model
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S
FA10 2x2	F35	1.00	0.00	900.00	1.12	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		2.00	0.00	800.00	1.90	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		3.00	0.00	1100.00	2.49	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		4.00	0.00	1100.00	2.12	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		5.00	0.00	1100.00	2.38	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		6.00	0.00	1100.00	2.23	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		7.00	0.00	1100.00	1.76	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		8.00	0.00	1000.00	1.71	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		9.00	0.00	1000.00	1.79	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		10.00	0.00	1100.00	1.40	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
	F36	1.00	0.00	900.00	3.53	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		2.00	0.00	900.00	1.76	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		3.00	0.00	700.00	2.96	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		4.00	0.00	1000.00	2.60	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305
		5.00	0.00	800.00	2.36	2.72	1	0	317	0.01	102	0.76	88	88	1.60	0.79	2.27%	1305

Please note that only the first 15 rows of the data set were shown above. There were a total of 1572 rows in the actual spreadsheet used for the final regression analysis. The data used throughout this regression analysis consisted of 51 independent test vehicle/material set/test condition combinations; many of these test vehicles had 30 replicates. A general test vehicle description is shown in the left most column (Column A). The column letter will be used for all of the outputs from Minitab. The test vehicles that were used for the analysis are detailed in sections 4.1.1.1 through 4.1.1.11. For each test vehicle that was tested, there were several boards (replicates). The specific board # is listed in Column B. On each of the boards there were several test sites, the test site

number is shown in the next column (Column C). The fourth column from the left (Column D) was for substrate metallization which was entered as a categorical variable (also referred to as a dummy variable) this was either a 0 for the OSP substrate metallization or a 1 for the Ni/Au metallization. The next column (Column E) gives the interval where the component failed. If the number in this column is 900 it means that the component failed somewhere between 800 and 900 cycles, since interval readouts were taken every 100 cycles. The percent area of voiding was listed in Column F; this was calculated using digital image analysis software on a Sonoscan 6000. The percent area of voiding was calculated post-reflow, pre-accelerated life testing. The “frequency of cycles per hour’ was the number of cycles per hour that the boards experienced in accelerated life testing, this was the actual number of cycles per hour including transfer times between the thermal zones. The next two columns (Columns H & I) are categorical variables first the die classification, perimeter or area array and second, the die size, 5mm or 10mm. In Column J, the number of I/O on the die was detailed for the test vehicles: 317 for an FA10-2x2, 1268 for an FA10 4x4, 112 for a PB6 2x2, 88 for a PB8 2x2, 352 for a PB8 4x4. Column K listed the average pad opening area. To calculate this number, 30 pads were measured on each of the circuit boards for each of the metallizations for test vehicles 4.1.1.1 thorough 4.1.1.4, and an average pad area was used in the predictor column above. For test vehicles described in Sections 4.1.1.5-4.1.1.11 the area was calculated based on the measurements given by Colella and Thorpe [Colella, 2004; Thorpe, 1999]. The UBM diameter was provided by the flip chip manufacturer for all of the die, this was used to calculate the area of the UBM. The next column is an area ratio of the UBM area to the wettable pad area. Columns N-P are the material properties

(CTE, Tg and Modulus) of the underfill material used in the assembly. Board thickness was measured in mm. The last two columns of the spread sheet correspond to the calculation of inelastic strain (Column R) and the prediction of cycles to failure (Column S) from the analytical model that was developed in Section 5.2. Please refer to this section for the specific equations.

The first step in the regression analysis was to try and remove all variables that were either highly correlated or had a high p-value meaning they were not good predictors of reliability performance. A regression analysis was run using Minitab Statistical Analysis Software Version 13.0. To run a regression analysis, first cut and paste all of the columns of predictors from the table above into Minitab. Minitab was only used to run the regression analysis; Microsoft Excel was used for manipulation of numbers and data logging. The menu path used for the regression was: Stat(on the main menu bar)→Regression → Regression. Once the regression window pops up choose the ‘response’ (which was the ‘failed at’ column, Column E) and then the predictors (which were: site, metallization, voiding percentage, frequency, perimeter vs. area array, die size, number of I/O, the area ratio, CTE of underfill, Tg of underfill, Modulus of underfill, board thickness, and total strain from analytical model). While in the same regression window click ‘options’→Variance Inflation Factors→OK; the variance inflation factor (VIF) is used to detect whether one predictor has a strong linear association with the remaining predictors (the presence of multicollinearity among the predictors). VIF measures how much the variance of an estimated regression coefficient increases if your predictors are correlated (multicollinear) [Minitab, Inc., 2000]. If the VIF was greater than 10, the predictor was removed from the model. The initial data set that was investigated was for

test vehicles was 1160 data points, and corresponded to the test vehicles described in Sections 4.1.1.1-4.1.1.5. The reason that the test vehicles 4.1.1.6 through 4.1.1.11 were added in the initial regression analysis was because the percentage area of voiding was not available for the later set of test vehicles. The desired output of multiple linear regression is $y_i = \beta_o + \beta_1 x_{1i} + \dots + \beta_k x_{ki} + e_i$. The coefficients $\beta_o, \beta_1, \dots, \beta_k$ (which are shown in the second column below) were unknown parameters and they were estimated by the method of least squares. The output from the regression analysis is shown in the table below:

Table B-3 Initial Regression Output: to illustrate the p-value and VIF output for the predictors

Predictor	Coefficient	SE Coef	T	P-Value	VIF
Constant	-959	653.4	-1.47	0.142	
C	1.508	4.881	0.31	0.757	1.1
D	762.26	40.86	18.66	0	1.8
F	-30.521	9.143	-3.34	0.001	3.2
G	207.88	10.02	20.74	0	1.2
H	2225.3	931.5	2.39	0.017	951.5
I	-2431	3367	-0.72	0.47	8333.8
J	1.962	3.55	0.55	0.581	11359.4
M	1530.5	227.4	6.73	0	36.1
N	-61.134	6.063	-10.08	0	3
O	20.568	1.305	15.76	0	2.6
P	464.34	64.33	7.22	0	2.4
R	21649	6402	3.38	0.001	4.5

The table above shows that there is a strong correlation between some of the predictors: H,I,J and M (high VIF value). These are die size, number of I/O, perimeter vs. area array and, the area ratio in the solder joint. The regression analysis does not tell you how they are related or which of the variables is related to which other variable. So,

at this point, each of these needed to be removed one at a time and the analyses re-run with the remainder of the predictors until there are no predictors that are multicollinear. It is obvious that the first three predictors are strongly related so, both die size and perimeter vs. area array were removed from the model. After they were removed the regression analysis was re-run, and the results are shown in Table B-4.

Table B-4 Regression Output after Die Size and Bump Arrangement were Removed

Predictor	Coefficient	SE Coef	T	P	VIF
Constant	3623.70	788.10	4.60	0	
C	-5.73	6.14	-0.93	0.351	1.1
D	454.31	42.16	10.78	0	1.2
F	45.28	10.81	4.19	0	2.8
G	186.49	12.57	14.83	0	1.2
J	0.21	0.09	2.27	0.023	4.7
M	-598.30	108.90	-5.49	0	5.2
N	-60.03	7.60	-7.90	0	2.9
O	30.43	1.57	19.39	0	2.4
P	369.21	80.86	4.57	0	2.4
R	-33671.00	7442.00	-4.52	0	3.8

Next the Site number, C, was removed because it had a p-value greater than 10%, a modified table is shown below with the site number removed as a predictor.

Table B-5 Regression Output After C was Removed

Predictor	Coefficient	SE Coef	T	P	VIF
Constant	3639.50	787.80	4.62	0	
D	454.00	42.16	10.77	0	1.2
F	45.14	10.81	4.17	0	2.8
G	186.26	12.57	14.82	0	1.2
J	0.21	0.09	2.30	0.022	4.7
M	-603.20	108.80	-5.54	0	5.2
N	-60.54	7.58	-7.99	0	2.9
O	30.50	1.57	19.45	0	2.3
P	367.35	80.83	4.54	0	2.4
R	-33751.00	7441.00	-4.54	0	3.8

The next step was to use some informal diagnostics to evaluate the predictors since the p-values are all below 5% and the VIFs are all below 10. However, the values are greater than 1 so there is some correlation between variables; this will be addressed later in the discussion. The regression analysis outputs a regression equation for the above set of predictors. The equation is:

$$E = 3639 + 454D + 45.1F + 186G + 0.210J - 603M - 60.5N + 30.5O + 367P - 33751R$$

The coefficient for predictor F (which was voiding percentage) was + 45.1; so this means that increasing the voiding percentage will improve the life of the component. If this is taken to the extreme and you assume that the voiding percentage is 100%, meaning there was no underfill at all then the life of the component would be maximized at least in terms of this predictor. Underfill is obviously necessary to improve the fatigue life of a flip chip component; therefore, this prediction really doesn't make much sense. There is no formal diagnostic to check for this type of behavior. There are several informal diagnostics that could be used, one of which states "Estimated regression coefficients

with an algebraic sign that is opposite of that expected from the theoretical considerations or prior experience” [Neter, 1996]. Since voiding percentage is an important predictor and the effects of voiding are not accurately represented by the regression analysis, voiding was studied further with a small independent study where only the voiding percentage was changed. The substrate, reflow profile, etc. were all held constant and several assemblies were made with and without voiding to check for the effects of voiding on the reliability performance. The regression analysis was run on only FA10 2x2 chips with both Cu/Ni/Au and Cu/OSP substrate metallizations. Unfortunately, many of the predictors had to be removed since they were essentially constant (G, J and R). M was removed with a high p-value, and N and P were removed with high VIFs. What remained in the model was D, F, and O. The regression analysis showed that the voiding percentage did not have a statistical impact on reliability performance, with a final p-value of 16.1%, as shown in the table below.

Table B-6 Output Regression Analysis for the Voiding Study

Predictor	Coefficient	SE Coef	T	P-value	VIF
Constant	-345.6	303.1	-1.14	0.256	
D	1171	103.5	11.32	0	1.2
F	-46.29	32.89	-1.41	0.161	1.8
O	17.092	2.866	5.96	0	1.8

Based on the independent study of voiding percentage and the informal diagnostic analysis of the coefficient associated with voiding percentage in the initial regression analysis, voiding percentage was dropped as a potential predictor of reliability performance. Dropping the voiding percentage leaves D, G, M, N, O, P, R in the regression analysis. Since, voiding was determined to not be a reliability predictor of performance additional data was available for the modeling effort, namely for test

vehicles as described in Sections 4.1.1.6-4.1.1.11. The data for these test vehicles was added into the regression analysis. At this point it was decided that the frequency of cycles per hour, G, the coefficient of thermal expansion, N, and the modulus of the underfill layer, P, would not be appropriate predictors since their influence should be included in the prediction of the plastic strain range or the predicted number of cycles to failure by the analytical model. The frequency in cycles per hour is included in the calculation for single power law creep, it is the time in the hot zone of the thermal cycle. The coefficient of thermal expansion and the modulus of the underfill were included in the calculation of time-independent plastic strain. This left D, M, O, R in the regression analysis. The discussion of why these variables are important is given in detail in Section 5.2.6. However the final output of the regression analysis is shown below:

Table B-7 Output of Regression Data with all Test Vehicles Included [R-squared 30.6%]

Predictor	Coefficient	SE Coef	T	P	VIF
Constant	2501.7	129.7	19.29	0	
D	451.03	37.63	11.99	0	1.1
M	-938.8	48.91	-19.19	0	1.2
O	2.4226	0.8401	2.88	0.004	1.5
R	-27907	3861	-7.23	0	1.1

The next step in the modeling effort was to manipulate the final form of the equation into the format that was desired. Fatigue strengths or endurance limits are modified to account for physical differences between the actual parts in use and the parts that were used to obtain the fatigue data. Types of correction factors include those for: differences in loading conditions, temperature differences, and surface finish on machined specimens. An example of an endurance limit with correction factors is given by Equation B-1 [Norton, 2000].

$$S_e = C_{load} C_{size} C_{surf} C_{temp} C_{reliab} S_e' \quad (B-1)$$

The term with the prime is the unmodified endurance limit and the term without the prime is the modified endurance limit. The above equation is intrinsically linear, which means that multiple linear regression can be used to fit the correction factors with the appropriate mathematical manipulation.

The predictors that are left in the model are metallization, which is a categorical variable, the glass transition temperature of the underfill material, and the area ratio of the final solder joint shape (as well as either the inelastic strain range or the predicted number of cycles to failure). Since the metallization is a categorical variable, which has been defined as a 0 for the Cu/Ni/Au substrate metallization and a 1 for the Cu/OSP metallization, it is important to appropriately define the metallization term such that the variable does not go to zero when there is a Cu/Ni/Au substrate. Another consideration is that for an unmodified number of cycles to failure (as calculated by the analytical model) an exponent is not desired on the term, N_f' , such that it maintains the form as specified in Equation B-1. To account for the final form of the equation, the variables were manipulated such that they looked like the following table (note that the first 7 rows are shown in the table for illustrations purposes, however the table is 1572 lines long). If a term is desired in the exponent like metallization in Equation B-3 it is entered into the chart as is, if the term is desired with an exponent like the area ratio of the solder joint shape in Equation B-4 then you must run the regression analysis with the natural log of the original value.

Table B-8 Converted Values of the Predictors for the Final Regression

Metal	ln(experimental failure times)	ln(A/A)	ln(Tg)	ln(predicted cycles to failure)	ln(total strain)	ln(experimental/predicted)
D	ln(E)	ln(M)	ln(O)	ln(S)	ln R	ln(E/S)
0.000	6.802	-0.279	4.477	7.174	-3.784	-0.372
0.000	6.685	-0.279	4.477	7.174	-3.784	-0.489
0.000	7.003	-0.279	4.477	7.174	-3.784	-0.171
0.000	7.003	-0.279	4.477	7.174	-3.784	-0.171
0.000	7.003	-0.279	4.477	7.174	-3.784	-0.171
0.000	7.003	-0.279	4.477	7.174	-3.784	-0.171
0.000	7.003	-0.279	4.477	7.174	-3.784	-0.171

A regression analysis was once again run, but this time with the converted variables. The variables were first run with the plastic strain range which gave the following output:

Table B-9 Regression Output for Low Cycle Strain Based Fatigue Equation with Correction Factors

The regression equation is:					
ln(E) = - 1.51 + 0.531D-1.23ln(M)+0.756ln(O)-1.29lnR					
Predictor	Coefficient	SE Coef	T	P	VIF
Constant	-1.5058	0.5227	-2.88	0.004	
D	0.5310	0.0361	14.72	0	1.1
ln(M)	-1.2326	0.0515	-23.94	0	1.3
ln(O)	0.7559	0.0697	10.85	0	1.4
ln R	-1.2898	0.0995	-12.97	0	1

It should be mentioned that the conversion of the factors to a multiplicative form increased the R-squared value from 30.6% to 44.3%. This means that

additional variability was explained by the model and therefore the predictive capability of the model was enhanced with the conversion to a multiplicative form. Now, to convert the above regression output (refer to equation in Table B-9) into the final form by mathematically manipulating the output to get rid of the natural logs (take the exponent of both sides). This gives the following equation:

$$E = 0.22 \cdot 1.70^D \cdot M^{-1.23} O^{0.756} R^{-1.29} \quad (B-2)$$

Placing the actual variables back into the expression above results in the following final form of the equation:

$$N_f = C_{\text{metallization}} (\text{Pad finish}) \cdot C_{\text{joint shape}} (A_{\text{UBM}}, A_{\text{Pad}}) \cdot C_{T_g} (\text{Underfill}) \cdot \Delta\gamma_p^{-1.29} \quad (B-3)$$

Where,

$$C_{\text{metallization}} = 0.22 * 1.70^M$$

The term metallization refers to the metallization of the substrate bond pads, where M is 0 for a Cu/Ni/Au finish and M is 1 for a Cu/OSP substrate bond pad finish.

$$C_{\text{joint shape}} = \left[\frac{A_{\text{UBM}}}{A_{\text{Pad}}} \right]^{-1.23} \quad (B-4)$$

A_{UBM} , is the area of the under bump metallurgy and A_{pad} is the wettable pad area on the substrate.

$$C_{T_g} = T_g^{0.76} \quad (B-5)$$

Where T_g is the glass transition temperature of the underfill material that is sandwiched between the silicon die and the substrate. The total plastic strain in one thermal cycle is given by $\Delta\gamma_p$.

The final regression plots for the model are shown below:

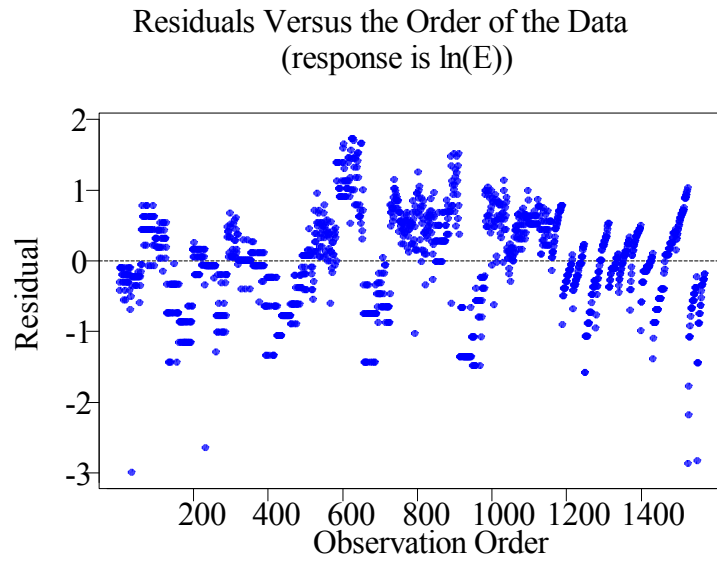


Figure B-2 Residuals vs. Order of the Data (for the strain based fatigue model)

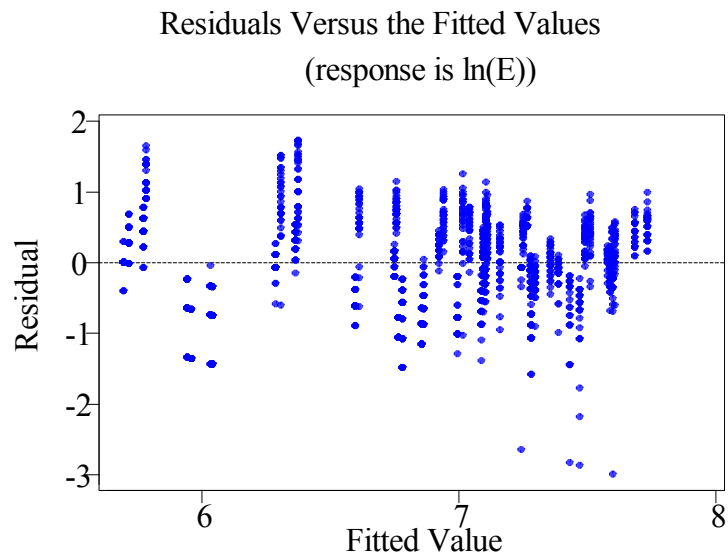


Figure B-3 Residuals vs. Fitted Values (for the strain based fatigue model)

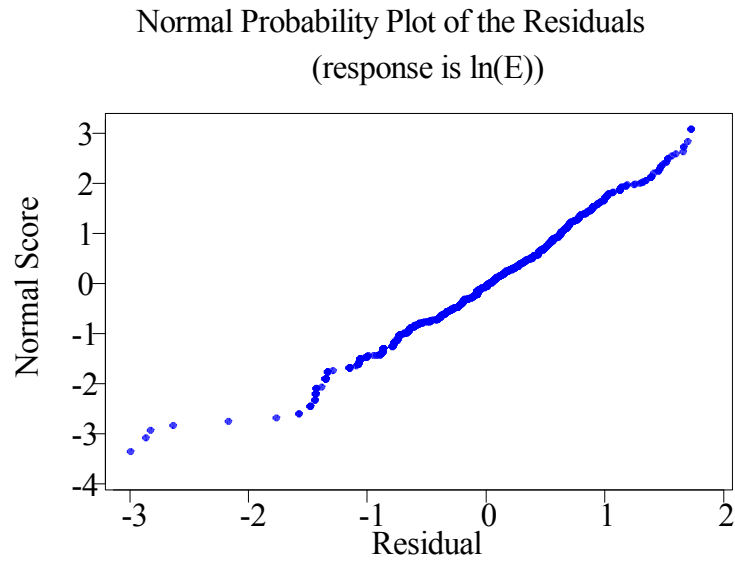


Figure B-4 Normal Probability Plot of Residuals (for the strain based fatigue model)

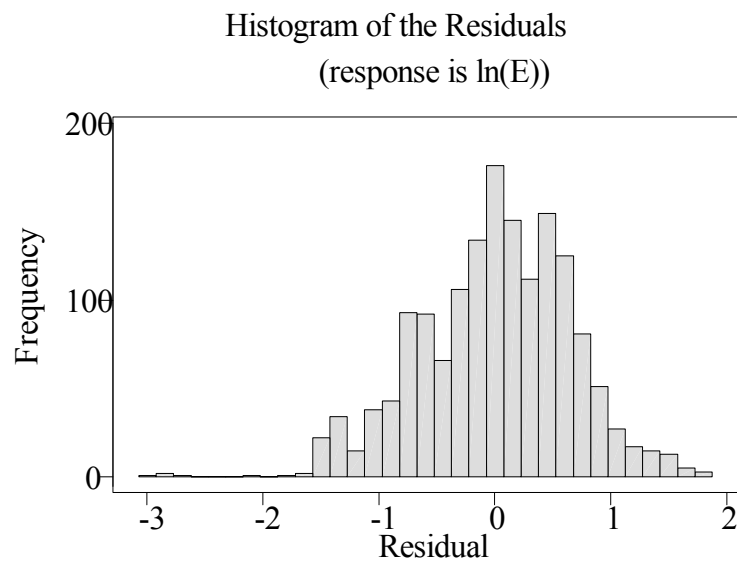


Figure B-5 Histogram of the Residuals (for the strain based fatigue model)

Finally, the regression analysis was also run such that a model could be generated with the following form:

$$N_f = C_1 C_2 \dots C_n N_f' \quad (B-6)$$

The output of this regression analysis is shown in the table below:

Table B-10 Regression Output for the Modified Cycles to Failure Approach

The regression equation is:					
$\ln(E/S) = -3.27 + 0.438D - 1.21\ln(M) + 0.679\ln(O)$					
Predictor	Coefficient	SE Coef	T	P	VIF
Constant	-3.266	0.328	-9.970	0	
D	0.438	0.038	11.550	0	1.1
$\ln(M)$	-1.211	0.054	-22.250	0	1.3
$\ln(O)$	0.679	0.073	9.360	0	1.4

It should be mentioned that the conversion of the factors to a multiplicative form increased the R-squared value from 30.6% to 37.8%. This means that additional variability was explained by the model and therefore the predictive capability of the model was enhanced with the conversion to a multiplicative form. Now, to convert the above regression output into the final form by mathematically manipulating the output to get rid of the natural logs (take the e of both sides). This gives the following equation:

$$N_f = C_{\text{metallization}} (\text{Pad finish}) \cdot C_{\text{joint shape}} (A_{\text{UBM}}, A_{\text{Pad}}) \cdot C_{T_g} (\text{Underfill}) \cdot N_f' \quad (B-7)$$

Where,

$$C_{\text{metallization}} = 0.038 * 1.55^M \quad (B-8)$$

The term metallization refers to the metallization of the substrate bond pads, where M is 0 for a Cu/Ni/Au finish and M is 1 for a Cu/OSP substrate bond pad finish.

$$C_{joint\ shape} = \left[\frac{A_{UBM}}{A_{Pad}} \right]^{-1.21} \quad (B-9)$$

A_{UBM} , is the area of the under bump metallurgy and A_{pad} is the wettable pad area on the substrate.

$$C_{T_g} = T_g^{0.679} \quad (B-10)$$

Where T_g is the glass transition temperature of the underfill material that is sandwiched between the silicon die and the substrate. Recall, that N_f' is the unmodified fatigue life of the solder joints as predicted by finite element modeling or via an analytical approach.

The final regression plots for the modified cycles to failure model are shown below:

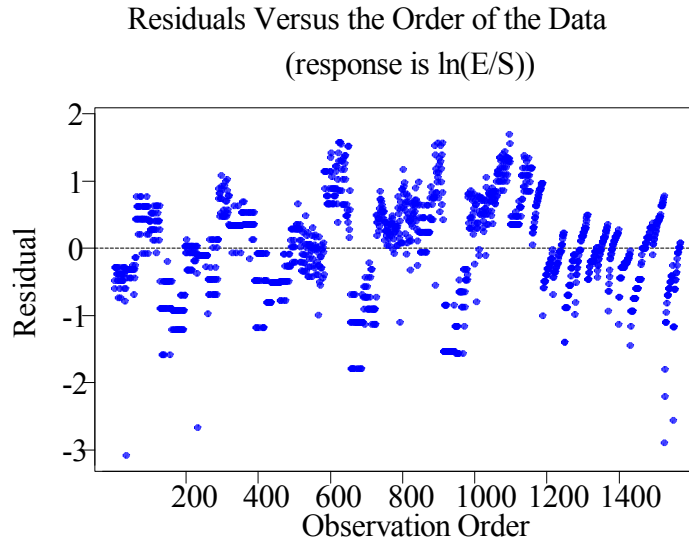


Figure B-6 Residuals vs. the order of the Data (for modified cycles to failure approach)

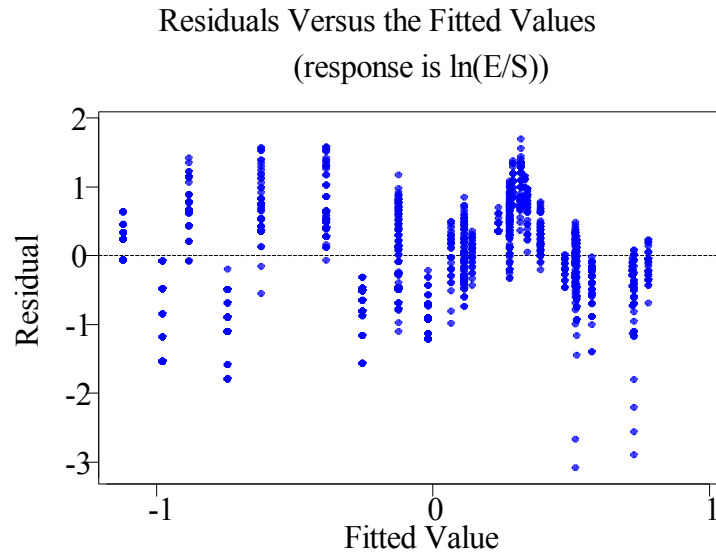


Figure B-7 Residuals vs. the Fitted Values (for modified cycles to failure approach)

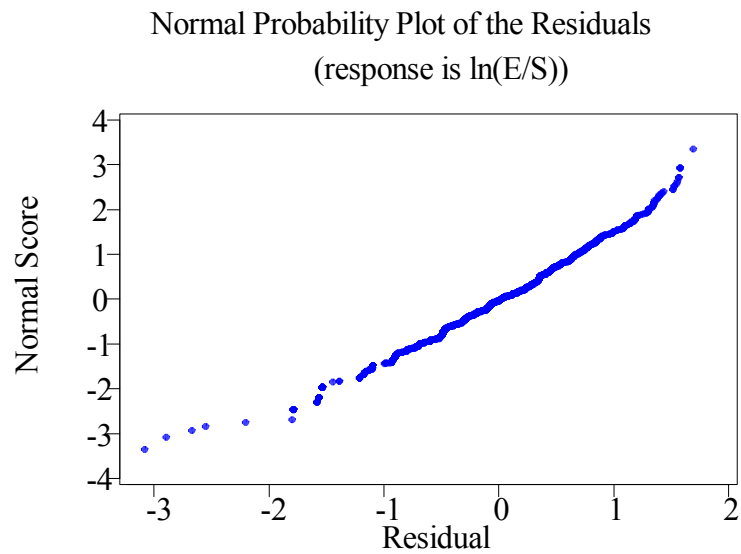


Figure B-8 Normal Probability Plot of the Residuals (for modified cycles to failure approach)

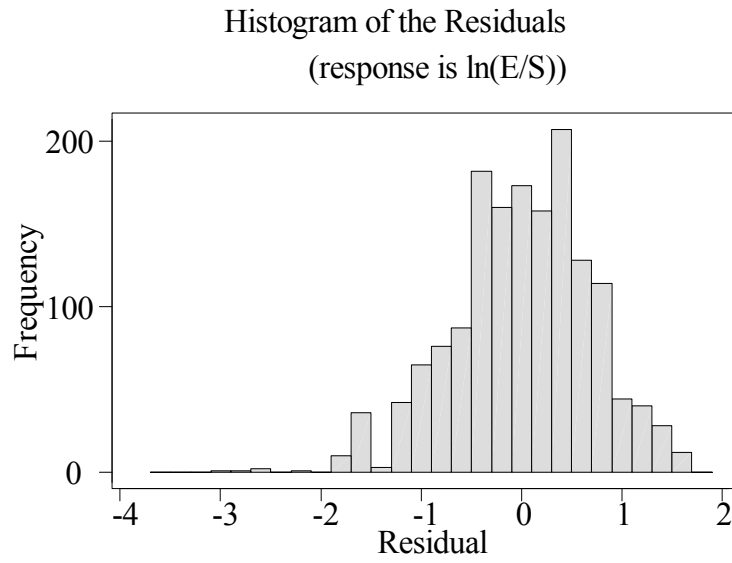


Figure B-9 Histogram of the Residuals (for modified cycles to failure approach)

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